Matrox Radient eCL

Installation and Hardware Reference

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Chapter 1

Introduction

This chapter briefly describes the features of the Matrox Radient eCL boards, as well as the software that can be used with the boards.

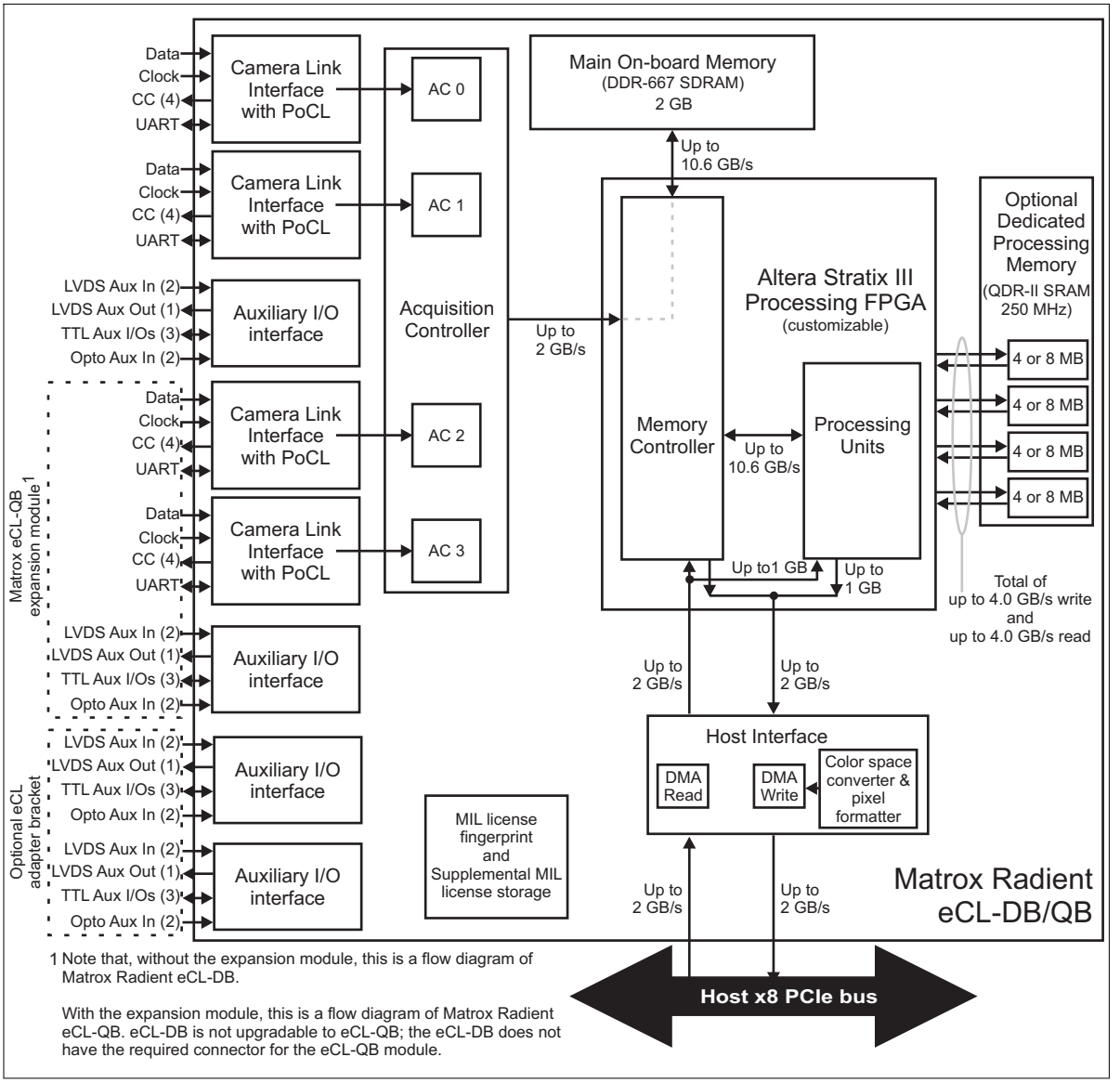
Matrox Radient eCL boards

Matrox Radient eCL is a family of high-performance PCIe frame grabbers that acquire images from Camera Link video sources and offer FPGA-based processing offload capabilities.

There are four Matrox Radient eCL members: eCL-DB, eCL-QB, eCL-SF, and eCL-DF. Matrox Radient eCL-DB and eCL-QB support acquisition from Camera Link video sources in Base configuration; eCL-DB supports simultaneous acquisition from two of these video sources, whereas eCL-QB supports four simultaneously. Matrox Radient eCL-SF and eCL-DF support acquiescing from Camera Link video sources in Medium or Full configuration (with up to 10 taps); eCL-SF supports acquisition from one of these video sources, whereas eCL-DF supports two simultaneously.

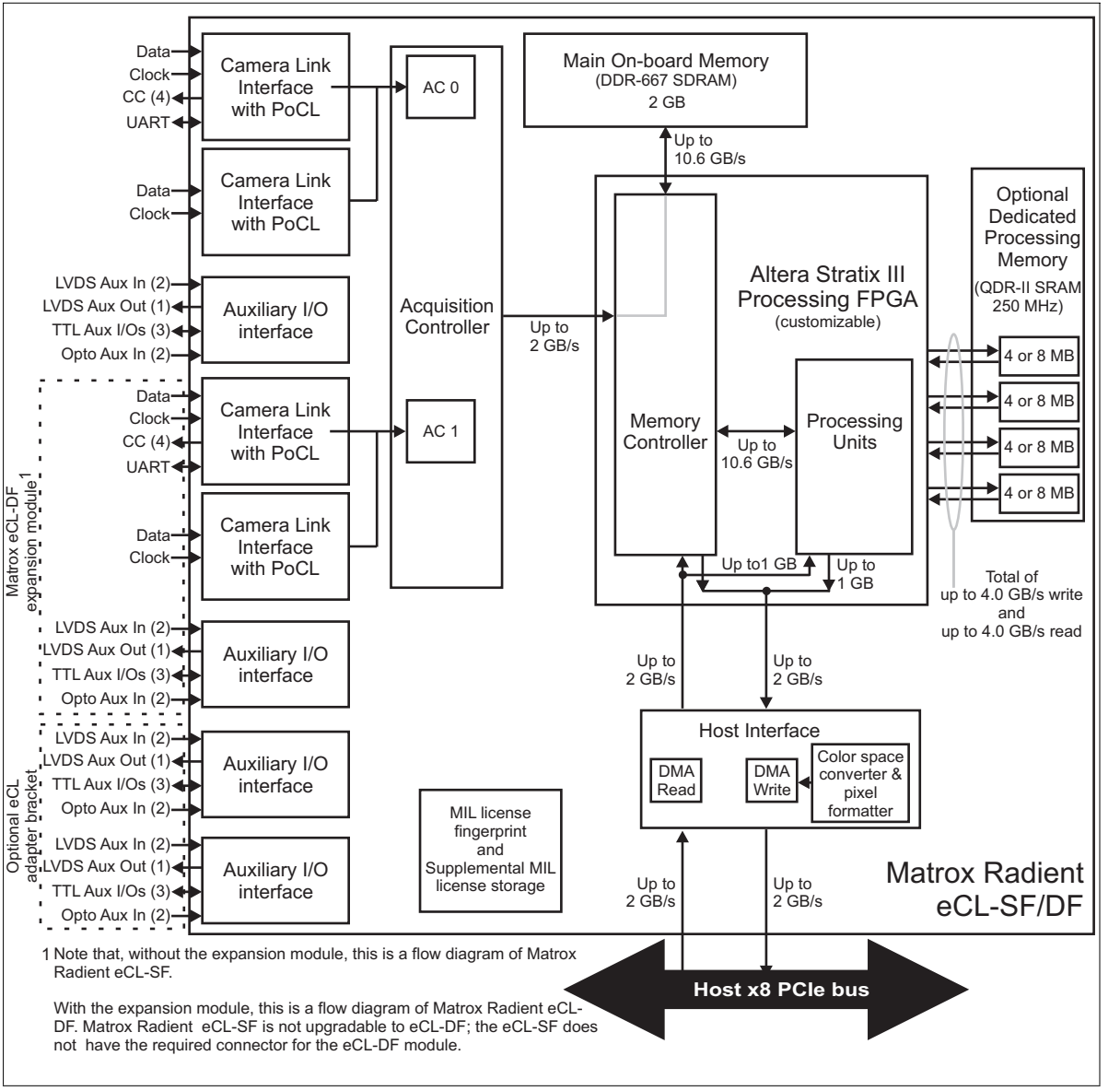
Matrox Radient eCL supports power-over Camera Link (PoCL) compliant video sources and Camera Link frequencies of 20 MHz to 85 MHz.

This manual uses the term Matrox Radient eCL to refer to all members of Matrox Radient eCL. It uses the term Matrox Radient eCL-DB/QB to refer to both Matrox Radient eCL-DB and eCL-QB. It uses the term Matrox Radient eCL-SF/DF to refer to both Matrox Radient eCL-SF and eCL-DF. When necessary, this manual distinguishes between the boards using their full names.



1 Note that, without the expansion module, this is a flow diagram of Matrox Radient eCL-DB.

With the expansion module, this is a flow diagram of Matrox Radient eCL-QB. eCL-DB is not upgradable to eCL-QB; the eCL-DB does not have the required connector for the eCL-QB module.



1 Note that, without the expansion module, this is a flow diagram of Matrox Radient eCL-SF.

With the expansion module, this is a flow diagram of Matrox Radient eCL-DF. Matrox Radient eCL-SF is not upgradable to eCL-DF; the eCL-SF does not have the required connector for the eCL-DF module.

General acquisition features

Matrox Radient eCL supports frame and line-scan monochrome and color video sources. The color video sources can be RGB video sources or video sources with a Bayer color filter. Matrox Radient eCL can decode Bayer color-encoded images on-board if the selected Processing FPGA configuration supports Bayer color decoding and the decoding supports the image size and depth; the standard FPGA configuration supports Bayer color decoding. Besides standard Camera Link video sources, Matrox Radient eCL also supports additional types of video sources, including some time-multiplexed video sources and 10-tap 8-bit video sources.

Processing capabilities

Matrox Radient eCL features an on-board real-time processing FPGA device, which can be configured to offload and even accelerate the most compute-intensive part of typical image processing applications, without generating additional data traffic within the host computer (Host).

Processing FPGA

The Processing FPGA on Matrox Radient eCL is a highly customizable, Altera Stratix III or IV FPGA, with a core clock of up to 133 MHz. The operations performed on-board are controlled using the Matrox Imaging Library (MIL) application development software. Using MIL, the processing units (PUs) of an FPGA configuration can be rearranged to perform the operations in the required sequence, without having to necessarily generate a new FPGA configuration. When the need arises, Matrox's FPGA design services can be employed to generate an application-specific FPGA configuration.

Before the Processing FPGA can process grabbed images, they must be stored in main on-board memory. If images stored in Host memory are required, they can be streamed directly to the Processing FPGA for processing. Images resulting from Processing FPGA processing can be stored in main on-board memory or streamed to the Host.

On-board acquisition and processing memory

Matrox Radient eCL has two types of on-board memory: main on-board memory and dedicated Processing FPGA memory (optional).

Main on-board memory is used to store acquired images, and images for or resulting from processing. As main on-board memory, Matrox Radient eCL is equipped with 2 Gbytes of DDR2-667 SDRAM. Main on-board memory is accessed through the memory controller of the Processing FPGA. The memory controller has multiple input ports and a data transfer rate of up to 10.6 Gbytes/sec.

Matrox Radient eCL can optionally feature dedicated Processing FPGA memory to store intermediate data while the Processing FPGA performs operation. As Processing FPGA memory, Matrox Radient eCL uses 4 banks of QDR-II SRAM that total 16 or 32 Mbytes of memory and have a total transfer rate of up to 4.0 Gbytes/sec in each direction.

Additional functionality

In addition to the core video capture and processing capabilities, Matrox Radient eCL incorporates a variety of features to simplify overall system integration. These features include:

- **LVDS-compatible serial interfaces (1 for each acquisition path).** Each interface is mapped as a COM port so that it can be accessed through the Win32 API. The serial interface can both receive and transmit signals, in full-duplex (bidirectional) mode.

- **Color space converter and pixel formatter.** These can convert captured or processed data as it is being transferred to the Host. They can convert 8- or 16-bit monochrome or 24- or 48-bit packed BGR data to monochrome, packed BGR, packed BGRa, planar RGB, or YUV (YUYV) format. In addition, they can flip, crop, or subsample data sent to the Host.

- **Auxiliary, multi-purpose signals.** These are non-video signals that can support one or more functionalities depending on the auxiliary signal (for example, trigger input or timer output). The number of signals each board supports is given in the table below.

Board	Auxiliary signals available
Matrox Radient eCL-DB	8 + 16* + (4 + 4)†
Matrox Radient eCL-SF	8 + 16* + (4)†
Matrox Radient eCL-QB	16 + 16* + (4 + 4 + 4+ 4)†
Matrox Radient eCL-DF	16 + 16* + (4 + 4)†

*. This is the number of auxiliary signals available when using the optional eCL-QB/DF cable adapter bracket.
†. These are the standard camera control signals available on the Camera Link connector(s).

- Integrated rotary decoders (2 for eCL-DB, 4 for eCL-QB, 1 for eCL-SF, 2 for eCL-DF). These can decode quadrature input received from a rotary encoder.

Data transfer

Under optimum conditions, Matrox Radient eCL can exchange data with the Host at a peak transfer rate of up to 2 Gbytes/sec, but can sustain a transfer rate of up to 1750 Mbytes/sec. Optimum conditions include using the board in a PCIe slot with 8 active lanes, using a 256-byte payload. DMA read and write performances are chipset and computer dependent, and are slightly affected by the image size and alignment in Host memory (frame start address and line pitch).

Software

To operate Matrox Radient eCL, you can use one or more Matrox Imaging software products that supports the board. These are the Matrox Imaging Library (MIL) and its derivatives (for example, MIL-Lite and Matrox Intellicam). All Matrox software is supported under Windows; MIL is also supported under Linux when using Matrox Radient eCL. Consult your software manual for supported versions of these operating systems.

MIL

MIL is a high-level programming library with an extensive set of optimized functions for image capture, processing, analysis, transfer, compression, display, and archiving. Image processing operations include point-to-point, statistical, spatial filtering, morphological, geometric transformation, and FFT operations. Analysis operations support calibration, are performed with sub-pixel accuracy, and include pattern recognition (normalized grayscale correlation and Geometric Model Finder), blob analysis, edge extraction and analysis, measurement, image registration, metrology, character recognition (template-based and feature-based), code recognition and verification (1D, 2D and composite code types), bead inspection, 3D reconstruction, and color analysis.

MIL applications are easily ported to new Matrox hardware platforms and can be designed to take advantage of multi-processing and multi-threading environments.

MIL-Lite

MIL-Lite is a subset of MIL. It includes all the MIL functions for image acquisition, transfer, display control, and archiving. It also allows you to perform processing operations that are typically useful to pre-process grabbed images.

Matrox Intellicam

Matrox Intellicam is an interactive Windows program that allows for fast video source interfacing and provides interactive access to all the acquisition features of your Matrox board. Matrox Intellicam also has the ability to create custom digitizer

configuration format (DCF) files, which MIL and its derivatives use to interface to specific non-standard video sources. Matrox Intellicam is included with all Matrox Imaging software products.

Essentials to get started

To begin using Matrox Radient eCL, you must have a computer with the following:

- An available conventional x8 (or x16) PCIe slot*. For Matrox Radient eCL-QB and eCL-SF, an additional adjacent slot is required (on the right of the slot when viewed from the back of the computer chassis); this slot need not be an electrical slot.
- Processor with an Intel 32-bit or 64-bit architecture, or equivalent.
- A relatively up-to-date PCIe chipset. The list of platforms that are known to be compatible with Matrox Radient eCL are available on the Matrox website, under the board's PC compatibility list.
- A proper power supply. Refer to the *Electrical specifications* section in *Appendix B: Technical information*.
- MIL or one of its derivatives. This software should be installed after you install your board.

*. Note that you can also install Matrox Radient eCL in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Radient eCL and the Host is reduced by 50%.

Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, the Matrox web site, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Consult your software package for other computer requirements (for example, operating system and memory requirements).

Inspecting the Matrox Radient eCL package

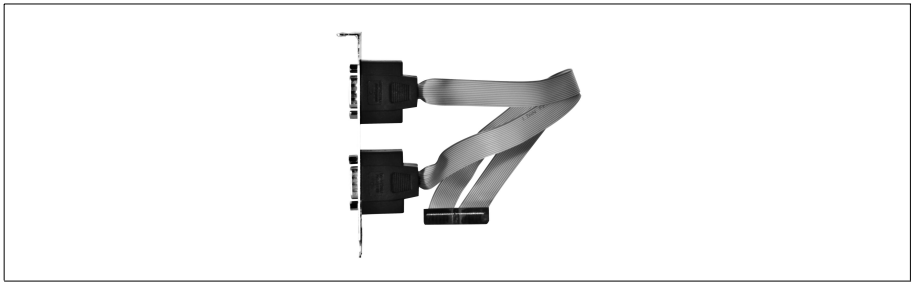
You should check the contents of your Matrox Radient eCL package when you first open it. If something is missing or damaged, contact your Matrox representative.

Standard items

You should receive the following items:

- The Matrox Radient eCL board, depending on which was purchased. If Matrox Radient eCL-QB or eCL-DF was purchased, the appropriate expansion module will be installed on the main board. Note that eCL-DB and eCL-SF are not upgradable to eCL-QB and eCL-DF, respectively; the eCL-DB and eCL-SF do not have the required connector for the expansion module.

- A Matrox Radient eCL cable adapter bracket with two DB-15 auxiliary I/O connectors. These connectors allow access from outside the computer enclosure to the auxiliary I/O signals of the internal auxiliary I/O connector.



Available separately

You might have also ordered one or more of the following:

- MIL or MIL-Lite. Matrox Intellicam is included with both of these software packages.

❖ If needed, you can purchase a 26-pin high-density male mini Camera Link or PoCL-compliant Camera Link cable (HDR or SDR) from the video source manufacturer, Components Express inc., 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties.

Handling components

The electronic circuits in your computer and the circuits on Matrox Radient eCL are sensitive to static electricity and surges. Improper handling can seriously damage the circuits. Be sure to drain static electricity from your body by touching a metal fixture (or ground) before you touch any electronic component. In addition, do not let your clothing come in contact with the circuit boards or components.

Warning

Before you add or remove devices from your computer, always **turn off** the power to your computer and all peripherals.

Installation

The installation procedure consists of the following steps:

1. Complete the hardware installation procedure described in *Chapter 2: Hardware installation*.

2. Complete the software installation procedure described in the documentation accompanying your software package.

More information

For information on using multiple Matrox Radient eCL boards, refer to *Chapter 3: Using multiple Matrox Radient eCL boards*.

For in-depth hardware information, refer to *Chapter 4: Matrox Radient eCL hardware reference*; whereas for a summary of this information, as well as environmental and electrical specifications, and connector pinout descriptions, see *Appendix B: Technical information*.

This manual occasionally makes reference to a MIL-Lite function. However, anything that can be accomplished with MIL-Lite can also be accomplished with MIL.

Need help?

If you experience problems during installation or while using this product, refer to the support page on the Matrox Imaging web site: www.matrox.com/imaging/support. This page provides answers to frequently asked questions, as well as offers registered customers additional ways of obtaining support.

If your question is not addressed and you are currently registered with the MIL maintenance program, you can contact technical support. To do so, you should first complete and submit the online Technical Support Request Form, accessible from the above-mentioned page. Once the information is submitted, a Matrox support agent will contact you shortly thereafter by email or phone, depending on the problem.

Chapter

2

Hardware installation

This chapter explains how to install your Matrox Radient eCL board in your computer.

Installing your Matrox Radient eCL board

Before you install your Matrox Radient eCL board, some precautionary measures must be taken. Turn off the power to your computer and its peripherals, and drain static electricity from your body (by touching a metal part of the computer chassis).

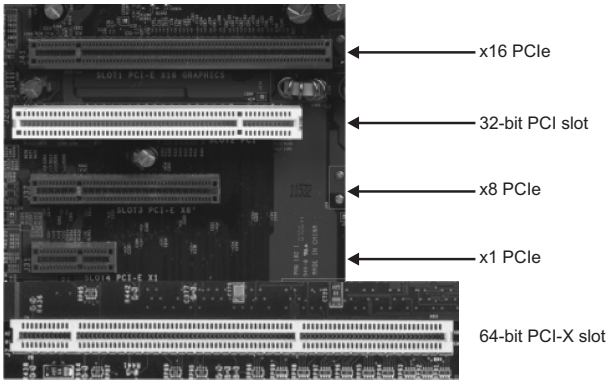
Important

❖ Note that your board should be installed before you install your software.

Proceed with the following steps to install your board:

1. Remove the cover from your computer; refer to your computer's documentation for instructions.

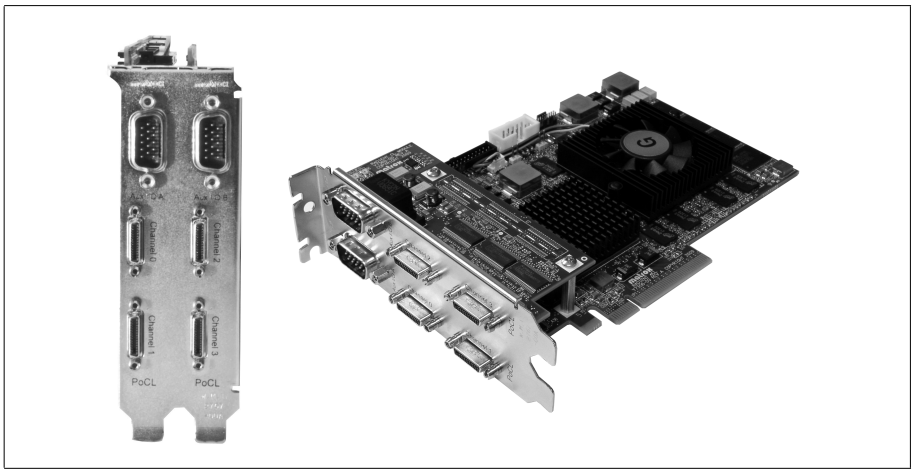
2. Check that you have an empty x8 (or x16) PCIe slot in which to install your Matrox Radient eCL*.



*. Note that you can also install Matrox Radient eCL in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Radient eCL and the Host is reduced by 50%.

Matrox Radient eCL might drop frames if there are not at least 8 active lanes on the PCIe connector to the Host (for example, if the board is connected to a x8 PCIe connector that has only four active lanes*). Verify with your motherboard manufacturer to find out whether your motherboard works efficiently with a x8 PCIe board, such as Matrox Radient eCL.

If installing Matrox Radient eCL-QB or eCL-DF, the slot immediately to the right of the selected slot must also be free. Matrox Radient eCL-QB and eCL-DF have a double bracket to accommodate the connectors on their main board and expansion module. Only the main board plugs into its slot's connector; the expansion module attaches only to the back of the computer's chassis.



If you need to install the cable adapter bracket of your Matrox Radient eCL board, you need an additional slot. This slot need not be adjacent to the Matrox Radient eCL board. In addition, the cable adapter bracket does not plug into the slot's connector; it attaches only to the back of the computer's chassis.

- Note that the external auxiliary I/O connectors on the cable adapter bracket are panel mount connectors. So if you don't want to occupy an entire slot to access the two connectors, you can punch out two holes in the computer chassis for these connectors, and then screw the connectors in the holes.

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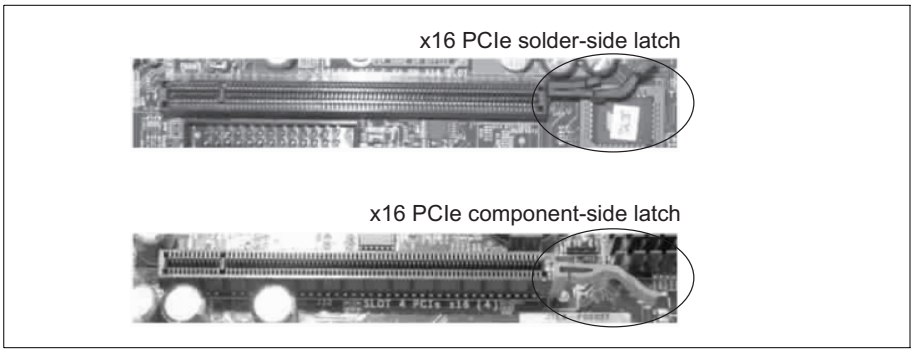
*. After installing the board, you can verify in software the number of PCIe lanes that are currently active using the MIL-Lite function MsysInquire() with M_PCIE_NUMBER_OF_LANES.

3. If there is a metal plate at the back of the selected slots, remove them. Keep the screw from the top of the plates to anchor your board and cable adapter bracket once they are installed.

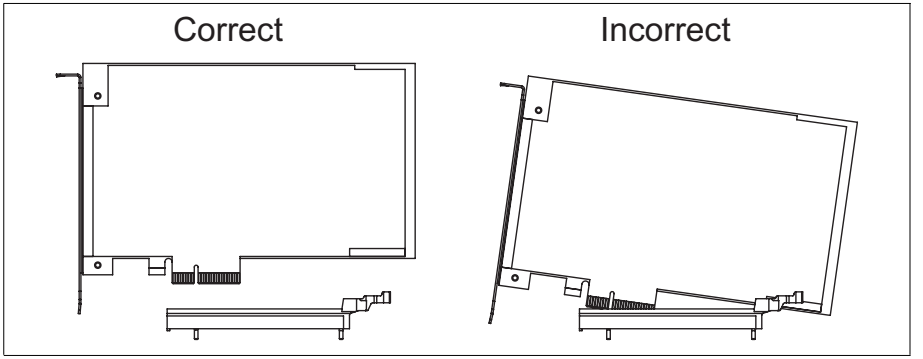
4. Position your Matrox Radient eCL board in the selected slot(s), and then press the board firmly but carefully into the connector of the slot.

Important

When installing your Matrox Radient eCL board in a x16 PCIe slot, special care must be taken to avoid damaging the board. Some x16 PCIe slots have a connector with a retainer. Matrox Radient eCL ***must not*** come into contact with the latch of this retainer.



The PCIe specification does not define appropriate keep-out regions for the latch to provide any tolerance to tilting or rotation when inserting or removing add-in boards in these connectors. Therefore, do not tilt the Matrox Radient eCL board backwards or rotate it when installing it; otherwise the board can touch the latch and get damaged. Note that the same is true when removing the board. Alternatively, you can remove the latch from the retainer.



5. Anchor the board using the screw that you removed in step 3.

6. If required, install the cable adapter bracket of your Matrox Radient eCL board, as described in the section *Installing the cable adapter bracket*, later in this chapter.

7. Attach your video sources, as described in the section *Connecting video sources*, later in this chapter.

Warning

- When connecting a video source in Full configuration, ensure that you are connecting its cables to the appropriate connector. Accidentally connecting the cables to the wrong connector can damage the board or your video source. Pins 2-5 and pins 15-18 are output pins on the top connector (0 and 2), while they are input pins on the bottom connector (1 and 3).

8. Turn on your computer.

   - When you boot your computer under Windows, Windows' Plug-and-Play system will detect a new Multimedia Video Device and you will be asked to assign it a driver. At this point, you should click on **Cancel**.

   Under Windows and Linux, the driver will be installed during the installation of Matrox Radient eCL software.

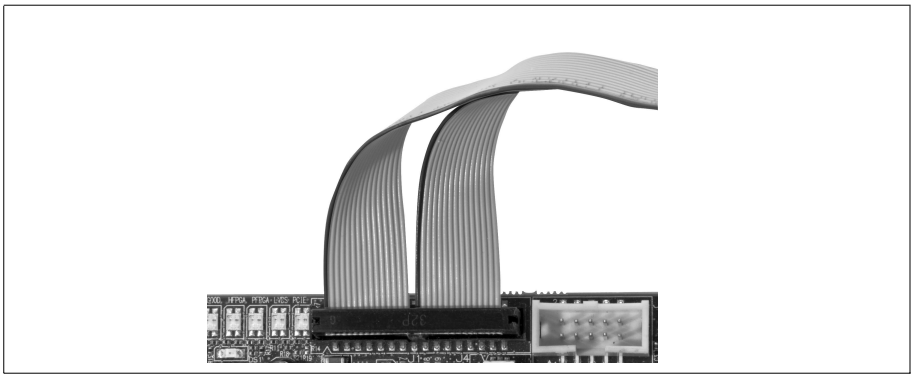
9. Under Windows, to maximize the performance of Matrox Radient eCL and to minimize the possibility of dropped frames, set the **Power Plan** option to **High Performance**.

Installing the cable adapter bracket

To install the cable adapter bracket of Matrox Radient eCL, proceed with the following steps:

1. Make sure that your Matrox Radient eCL board is fastened to the computer chassis.

2. Attach the cable adapter bracket's flat ribbon cable to the internal auxiliary I/O connector on the Matrox Radient eCL board. To do so, position the cable so that the black wire is on the same side as the bracket of the Matrox Radient eCL board.



3. Slide the bracket into the opening at the back of the selected slot.

4. Anchor the bracket to the chassis using the screw that you removed in the previous section.

Note that the external auxiliary I/O connectors on the cable adapter bracket are panel mount connectors. So if you don't want to occupy an entire slot to access the two connectors, you can punch out two holes in the computer chassis for these connectors, and then screw the connectors in the holes.

Connecting video sources

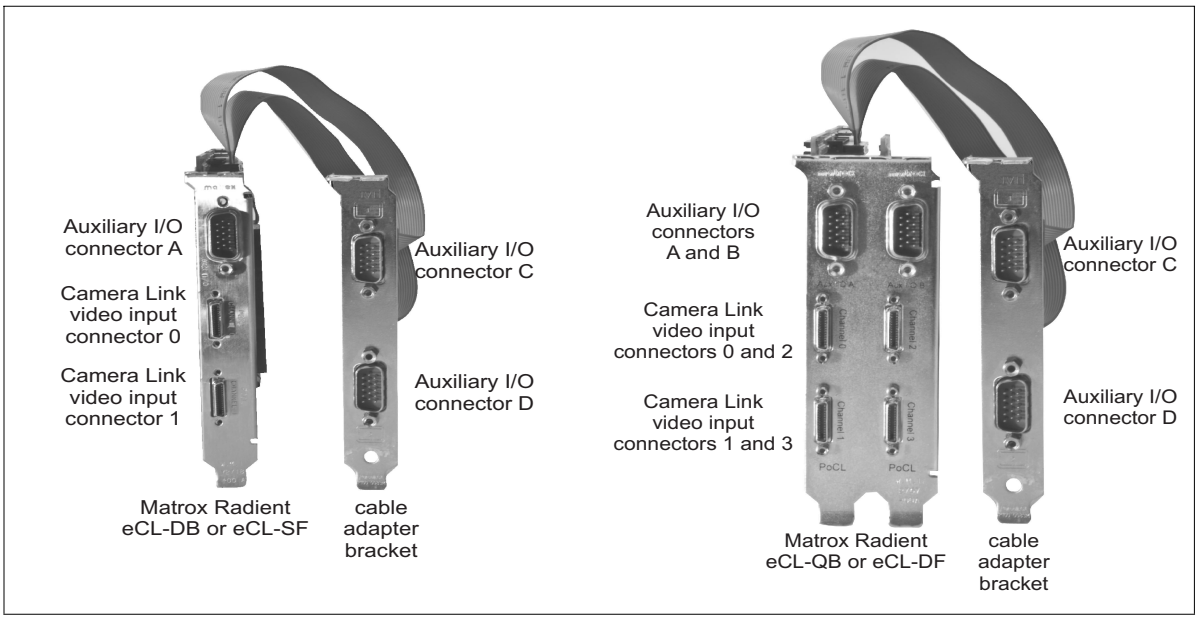
The Matrox Radient eCL board has the following connectors on its bracket(s):

- **Two or four Camera Link-compliant video input connectors.** Used to receive video input, timing, and synchronization signals, from the video source. These are also used to transmit/receive communication signals between the video source and the frame grabber.

- **External auxiliary I/O connector A or external auxiliary I/O connectors A and B (DBHD-15).** Each used to transmit/receive auxiliary signals.

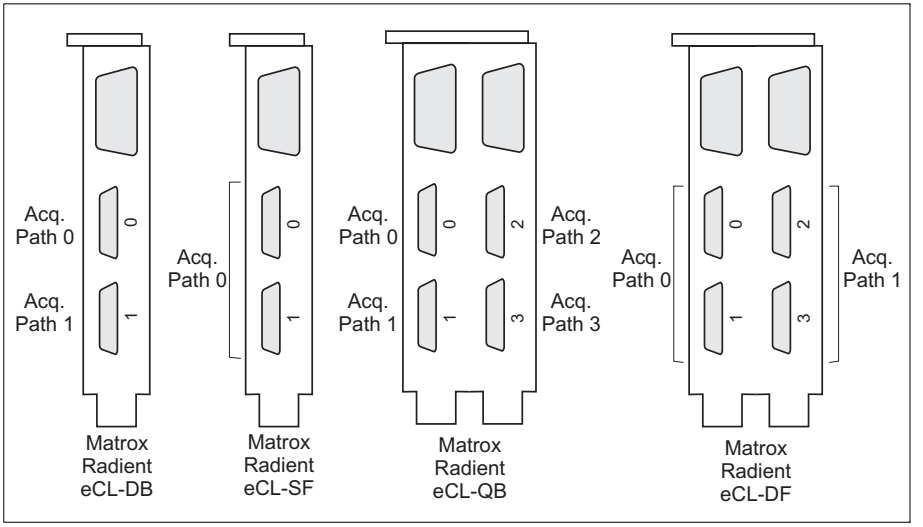
To access the signals of the internal auxiliary I/O connectors, you might have installed the cable adapter bracket. It has the following connectors:

- **External auxiliary I/O connector C and D (panel mount DBHD-15).** Each used to transmit/receive the auxiliary signals.



Attach video sources to Matrox Radient eCL as follows:

Matrox Radient board	Camera Link connector 0	Camera Link connector 1	Camera Link connector 2	Camera Link connector 3
eCL-DB	Video source 0 in Base configuration	Video source 1 in Base configuration	--	--
eCL-QB	Video source 0 in Base configuration	Video source 1 in Base configuration	Video source 2 in Base configuration	Video source 3 in Base configuration
eCL-SF	Video source 0 in Medium or Full configuration		--	--
eCL-DF	Video source 0 in Medium or Full configuration		Video source 1 in Medium or Full configuration	



Warning

❖ When connecting a video source in Full configuration, ensure that you are connecting its cables to the appropriate connector. Accidentally connecting the cables to the wrong connector can damage the board or your video source. Pins 2-5 and pins 15-18 are output pins on the top connector (0 and 2), while they are input pins on the bottom connector (1 and 3).

To connect video sources to the Camera Link connectors, use standard Camera Link cables with a 26-pin high-density male mini Camera Link connector (HDR or SDR) at one end. When connecting to PoCL-compliant video sources, you should use PoCL-compliant Camera Link cables (HDR or SDR). Camera Link cables are not available from Matrox; for possible sources, see the *Connectors on Matrox Radient eCL boards* section in *Appendix B: Technical information*.

❖ If using both Camera Link connectors to connect to the same video source (single-Medium mode or single-Full mode), the cables you choose must be of the same type and length. Otherwise, the cables can have different propagation delays.

Chapter

3

Using multiple Matrox Radient eCL boards

This chapter explains how to use multiple Matrox Radient eCL boards.

Installation of multiple boards

You can install and use multiple Matrox Radient eCL boards in one computer.

Install each additional Matrox Radient eCL board as you installed the first board (refer to *Chapter 2: Hardware installation*). The number of Matrox Radient eCL boards that you can install is primarily dependent on the number of physical slots in your computer and your BIOS; your BIOS establishes how many PCI devices can be mapped to the PCI memory space of your computer.

Using MIL-Lite, you have to allocate a MIL system for each board and allocate the resources of each MIL system. For more information, see **MsysAlloc**() with **M_SYSTEM_RADIENT** in the MIL Reference.

Simultaneous image capture from different boards

Besides simultaneously capturing images from multiple video sources attached to a Matrox Radient eCL board (except eCL-SF), you can simultaneously capture images from video sources attached to different Matrox Radient eCL boards. However, the number of video sources from which you can simultaneously capture images is computer-dependent.

The use of a high performance PCIe chipset is necessary to sustain PCIe transfers to Host memory. The list of platforms that are known to be compatible with Matrox Radient eCL are available on the Matrox web site, under the board's compatibility list.

To measure the effective, available bandwidth of the PCIe interface used by your Matrox Radient eCL board, you can use the RadientBench tool integrated in the MILConfig utility. As a reference point, capturing from a 2K x 2K, 8-bit, 60 frames/sec video source will require a minimum bandwidth of 240 Mbytes/sec, plus an additional bandwidth margin of approximately 20%, for a bandwidth of 288 Mbytes/sec.

Chapter

4

Matrox Radient eCL hardware reference

This chapter explains the architecture, features, and modes of the Matrox Radient eCL hardware.

Matrox Radient eCL hardware reference

This chapter provides information on the Matrox Radient eCL hardware. It covers the architecture, features, and modes of the board's acquisition section. In addition, the chapter covers the Matrox Radient eCL hardware related to the processing and transfer of data. A summary of the features of Matrox Radient eCL, as well as pin assignments for the various connectors, can be found in *Appendix B: Technical information*.

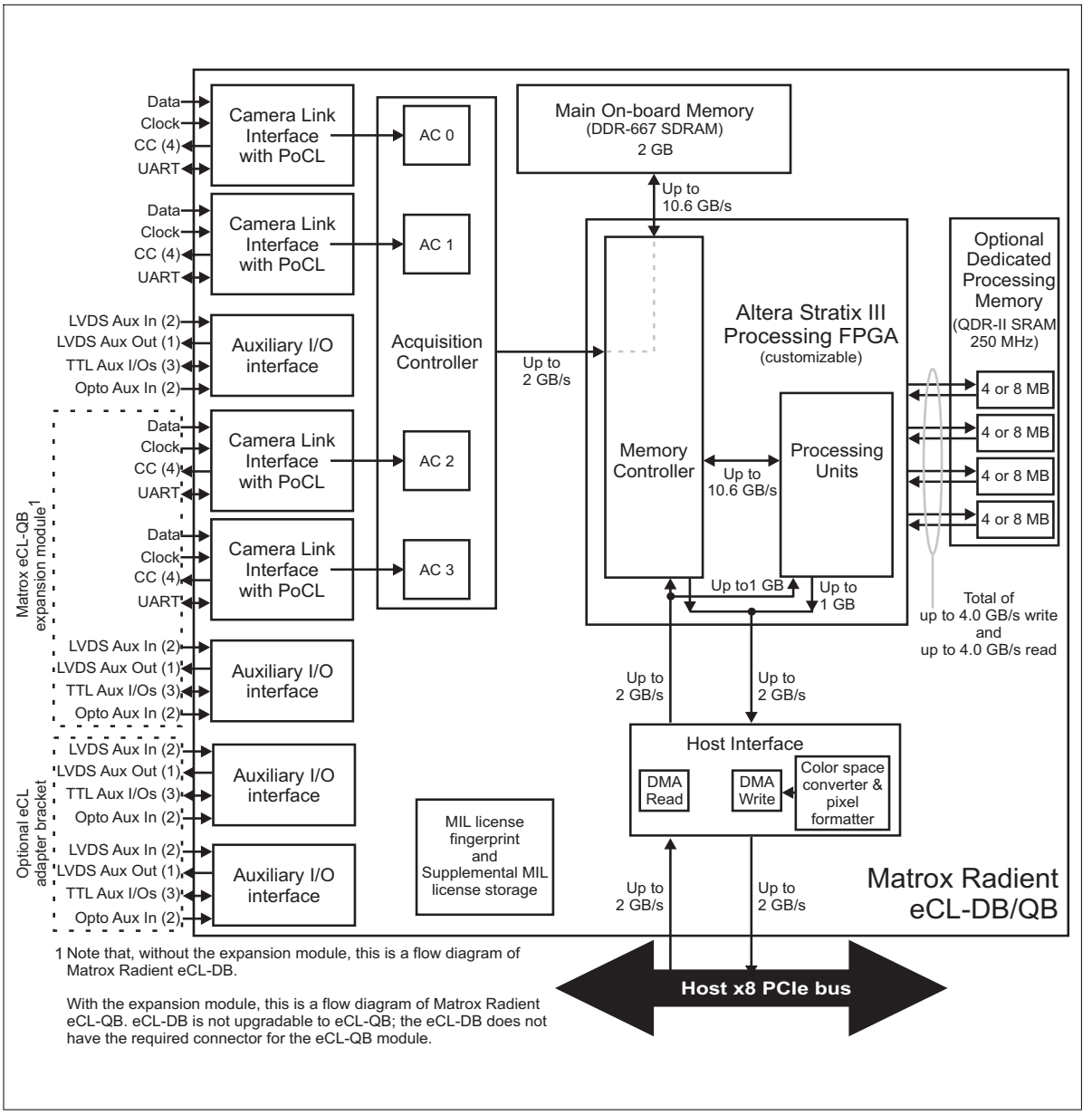
Acquisition path

This manual uses the term acquisition path to refer to a path that has the capability to, for example, capture a component or stream of the video input signal. The term *independent acquisition path* is used to refer to an acquisition path that can, if required, acquire data from a video source independently from another such path on the same frame grabber. Each independent acquisition path has its own programmable synchronization generator (PSG) to manage all video timing, synchronization, triggering, timer, and user input and output signals for the path.

MIL-Lite uses the concept of a MIL digitizer to represent the acquisition path(s) with which to grab from one input source of the specified type. When several MIL digitizers are allocated, their device number along with their DCF identify if they represent the same path(s) (but perhaps for a different input format) or independent path(s) for simultaneous acquisition.

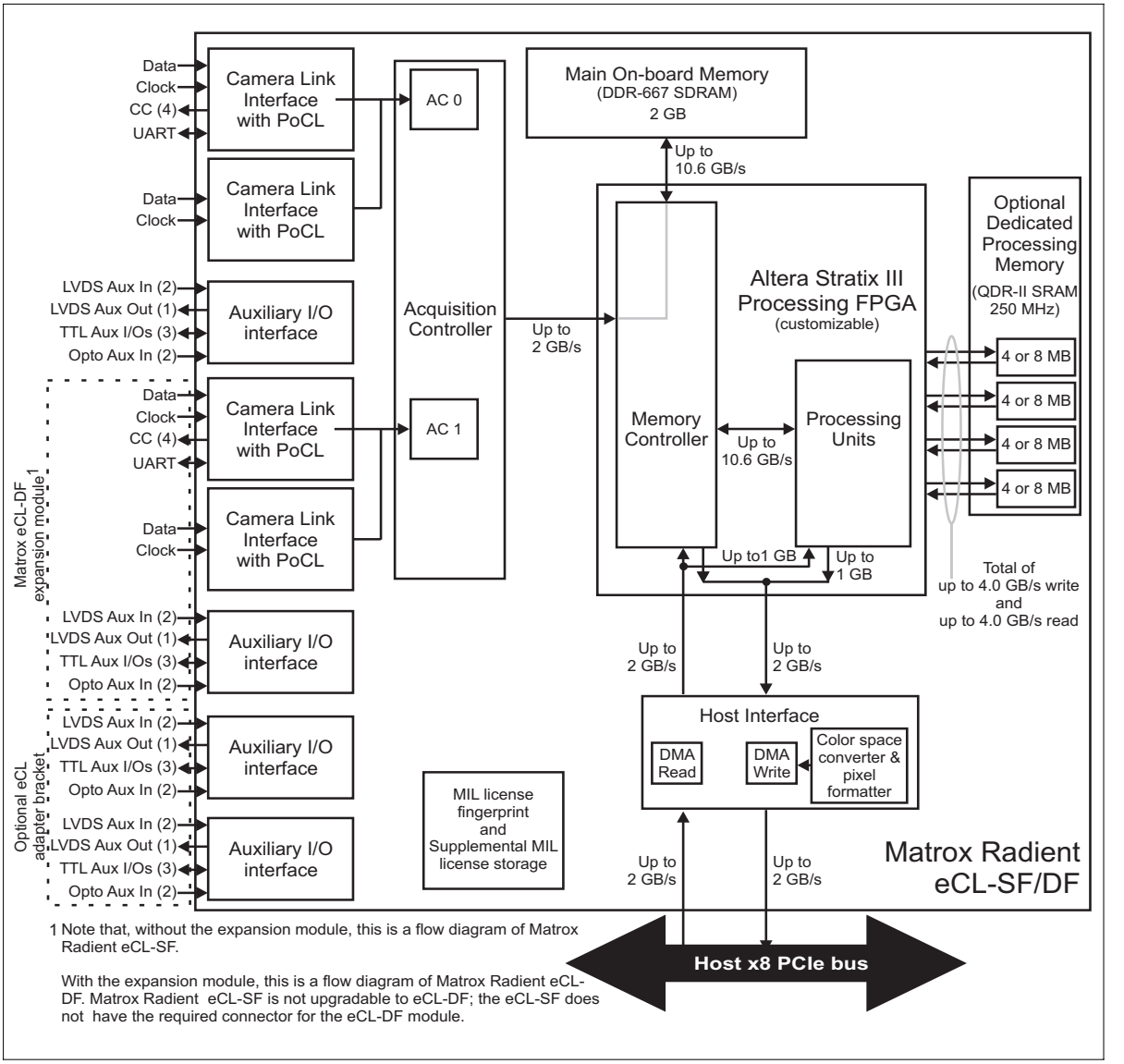
Digitizer configuration format

To program the acquisition section, allocate a MIL digitizer using **MdigAlloc**() with an appropriate DCF (supplied or created) and digitizer device number. If you find a DCF file that is suitable for your video source, but you need to adjust some of the more common settings, you can do so directly, without adjusting the file, using the appropriate MIL-Lite function. For more specialized adjustments, use the Matrox Intellicam program to adjust the DCF file. Using Matrox Intellicam, you can set the active video region, the sampling clock, and all the other parameters related to the timing of the video signal (that is, standard and non-standard video, interlaced or non-interlaced) in your DCF file.



1 Note that, without the expansion module, this is a flow diagram of Matrox Radient eCL-DB.

With the expansion module, this is a flow diagram of Matrox Radient eCL-QB. eCL-DB is not upgradable to eCL-QB; the eCL-DB does not have the required connector for the eCL-QB module.



1 Note that, without the expansion module, this is a flow diagram of Matrox Radient eCL-SF.

With the expansion module, this is a flow diagram of Matrox Radient eCL-DF. Matrox Radient eCL-SF is not upgradable to eCL-DF; the eCL-SF does not have the required connector for the eCL-DF module.

Matrox Radient eCL acquisition section

Matrox Radient eCL can capture video from digital video sources compliant with the Camera Link specification. Matrox Radient eCL can provide power over Camera Link to attached video sources.

Matrox Radient eCL supports monochrome, RGB color, and Bayer color-encoded acquisition. Matrox Radient eCL can decode Bayer color-encoded images on-board if the selected Processing FPGA configuration supports Bayer color decoding and the decoding supports the image size and depth; the standard FPGA configuration supports Bayer color decoding. Besides standard Camera Link video sources, Matrox Radient eCL also supports additional types of video sources, including some time-multiplexed video sources and 10-tap 8-bit video sources.

Matrox Radient eCL-DB has two independent acquisition paths in dual-Base mode, and Matrox Radient eCL-QB has four independent acquisition paths in quad-Base mode. Matrox Radient eCL-SF has one acquisition path in single-Full or single-Medium mode, and Matrox Radient eCL-DF has two acquisition paths in single-Full or single-Medium mode.

Each acquisition path can grab at Camera Link frequencies of 20 MHz to 85 MHz. Each acquisition path has its own programmable synchronization generator (PSG), and can have a different acquisition rate.

The acquisition section of Matrox Radient eCL supports a comprehensive set of general purpose I/O and serial ports to control cameras and other devices.

Performance

The video timing of each acquisition path is as follows:

	Maximum
Number of pixels / line (including sync and blanking)	64 K
Number of lines / frame (including sync and blanking)	64 K
Pixel clock	85 Mhz
Bandwidth	680 Mbytes/sec*

*. Matrox Radient eCL supports a bandwidth of 850 Mbytes/sec when grabbing from a 10-tap 8-bit camera at 85 MHz. In addition, Matrox Radient eCL can achieve up to 1750 Mbytes/sec total, depending on the DMA write performance of the board in your computer. When grabbing from 2 10-tap 8-bit cameras (1700 Mbytes/sec), you might have problems transferring images to the Host because the maximum bandwidth has been reached; this might cause you to miss frames.

The maximum pixel clock frequency is dependent on the length of the cable used. Refer to the *Technical features of Matrox Radient eCL* subsection of the *Board summary* section in *Appendix B: Technical information*.

Acquisition

A Base-type acquisition path supports a maximum of 24 bits of video data when acquiring from Camera Link-compliant video sources or up to 48 bits when acquiring from non-standard time-multiplexed video sources. Similarly, a Medium-type acquisition path can grab up to 48 bits of video data when acquiring from Camera Link-compliant sources or up to 64 bits when acquiring from non-standard time-multiplexed sources. Finally, a Full-type acquisition path supports up to 64 bits of video data when acquiring from Camera Link-compliant video sources and up to 80 bits when acquiring from non-standard video sources.

The video sources can be frame or line-scan video sources. Note that the acquisition paths in dual-Base, quad-Base, dual-Medium, and dual-Full mode are completely independent, and therefore the video sources do not need to be identical when running in these modes.

Supported video sources

Each acquisition path supports the following video sources:

	Video sources supported per acquisition path
Camera Link Standard	• One tap x 8/10/12/14/16-bit. • Two tap x 8/10/12-bit. • One tap 3 x 8-bit (RGB). • Four tap 8-bit with time-multiplexing.
Not Camera Link Standard	• Two tap 14/16-bit with time-multiplexing. • Four tap x 10/12-bit with time-multiplexing.

In addition to the above video sources, the following video sources are supported when running in single-Medium mode:

	Video sources supported
Camera Link Standard	• Four tap x 8/10/12-bit. • One tap 3 x 10/12-bit (RGB).
Not Camera Link Standard	• 8 tap x 8-bit with time-multiplexing (using only 2 receivers). • Two tap x 14/16-bit. • One tap 3 x 14/16-bit (RGB). • Two tap 3 x 8-bit (RGB) (genlocked).

In addition to the above video sources, the following video sources are supported when running in single-Full mode:

	Video sources supported
Camera Link Standard	• Eight tap x 8-bit. • 10 tap x 8-bit (sequential taps).
Not Camera Link Standard	• Four tap x 14-16-bit

Matrox Radient eCL supports power over Camera Link (PoCL) and non-PoCL compliant video sources. For compatibility with non-PoCL video sources, Matrox Radient eCL features SafePower mode to supply power only after determining whether the connected video source is PoCL compliant. The PoCL protection on-board fuse can sustain a current of 0.4 A.

ChannelLink receivers

Matrox Radient eCL uses ChannelLink receivers to grab from Camera Link video sources. Matrox Radient eCL-DB has two asynchronous ChannelLink receivers, permitting eCL-DB to operate in dual-Base mode; whereas Matrox Radient eCL-QB has four, permitting eCL-QB to operate in quad-Base mode. Matrox Radient eCL-SF has three ChannelLink receivers that can only operate synchronously. In single-Medium mode, Matrox Radient eCL-SF only uses two of the receivers, whereas in single-Full mode, it uses all three receivers. Matrox Radient eCL-DF has an additional three ChannelLink receivers that operate in the same manner as those on eCL-SF, permitting eCL-DF to operate in dual-Medium or dual-Full mode.

For Matrox Radient eCL-DB/QB, each ChannelLink receiver can receive up to 24 bits of video data and 4 bits of synchronization data from the video source, as serialized data over four LVDS pairs; a clock is received from the video source over a fifth LVDS pair.

For Matrox Radient eCL-SF, the first ChannelLink receiver has the same capabilities as the ChannelLink receivers on Matrox Radient eCL-DB/QB. In single-Medium mode, the second ChannelLink receiver can only receive up to 24 bits of video data and the third ChannelLink receiver is not used. In single-Full mode, the second and third ChannelLink receivers can each receive 28 bits of video data. The additional three ChannelLink receivers on Matrox Radient eCL-DF operate in the same manner as those on the eCL-SF.

The ChannelLink receivers can operate at frequencies of 20 MHz to 85 MHz.

Demultiplexers to support time-multiplexed video sources

Each acquisition path of the board features a demultiplexer. It can deserialize input from time-multiplexed video sources on a clock cycle basis. Time-multiplexed video sources can output larger pixel depths and more taps than are possible with non-time-multiplexed video sources in the same configuration (with the same amount of cabling). When enabled, the demultiplexer assumes that two video streams share the same data path and that the streams are interleaved based on the clock cycle. The demultiplexer assumes that on one clock cycle, the data is from one stream and that on the next clock cycle, the data is from another stream. The demultiplexer can only deserialize video inputs that, when combined and, if necessary, expanded, total a maximum depth of 64 bits per acquisition path.

Expansion refers to the automatic addition of padding zeros on the most significant bits (MSB) of 10-, 12-, and 14-bit data to create byte aligned 16-bit data. Expansion is not always necessary.

For each acquisition path, two LVDS pairs are used to transmit and receive asynchronous serial communication between the video source and the board. These signals are handled by the Universal Asynchronous Receiver/Transmitters (UARTs).

For each acquisition path, four camera control output signals are also available. These are general-purpose signals that are sent to the video source.

UARTs

For each acquisition path, Matrox Radient eCL offers an LVDS-compatible Matrox serial interface. Each interface is mapped as a COM port so that it can be accessed through the Win32 API. Each interface is comprised of both a transmit port and a receive port, permitting the interface to work in full-duplex (bidirectional) mode. The interfaces are located on the Camera Link connectors.

Each interface is controlled by a Universal Asynchronous Receiver-Transmitter (UART)[*]. Each UART features independently programmable baud rates, supporting all standard baud rates from 300 baud up to 115200[†] baud.

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*. The UART implementation was derived from a design by Daniel Wallner. Please see *Appendix C: Acknowledgments* for copyright information.

†. In addition, the maximum baud rate is highly dependent on the amount of computer resources available.

PSGs

For each acquisition path, Matrox Radient eCL features a programmable synchronization generator (PSGs). Each PSG allows for independent acquisition from one video source, since each PSG is responsible for managing all video timing and synchronization signals.

The PSGs are also responsible for managing the camera control and auxiliary signals supported by the board. These signals are configurable signals that can support one or several functions, one of which is user-defined; the table in the next subsection identifies the functions to which the camera control and auxiliary signals can be defined. The PSGs are also responsible for implementing the functionality to which these can be defined.

Camera control and auxiliary signals for Matrox Radient eCL-DB and eCL-QB

The following tables summarize the auxiliary functionality that the PSGs support, and the corresponding signals that the PSGs can receive/generate, for Matrox Radient eCL-DB and eCL-QB. The table also documents the MIL constants to use.

		LVDS cam. ctrl				LVDS cam. ctrl				LVDS cam. ctrl				LVDS cam. ctrl			
		Camera Link Connector 0				Camera Link Connector 1				Camera Link Connector 2*				Camera Link Connector 3*			
M_CC_IO*n*	n	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
for M_DEV*m*†	m	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
Functionality	Acquisition path	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4
Timer (M_TIMER*n*†)	0	1/2	1/2	1/2	1/2												
	1					1/2	1/2	1/2	1/2								
	2									1/2	1/2	1/2	1/2				
	3													1/2	1/2	1/2	1/2
User output (bit of Camera Link static-user-output register M_USER_BIT_CC_IO*n*†)	0	0/1	0/1	0/1	0/1												
	1					0/1	0/1	0/1	0/1								
	2									0/1	0/1	0/1	0/1				
	3													0/1	0/1	0/1	0/1

*. Only available on Matrox Radient eCL-QB

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

		TTL Aux I/O												OPTO Aux In								LVDS Aux In								LVDS Aux Out			
		Aux I/O Connector												Aux I/O Connector								Aux I/O Connector								Aux I/O Connector			
		A			C			B*			D			A		C		B*		D		A		C		B*		D		A	C	B*	D
M_AUX_IO*n*	n	8	9	2	8	9	3	8	9	2	8	9	3	6	7	0	1	6	7	0	1	10	11	4	5	10	11	4	5	12	12	13	13
for M_DEV*m*†	m	0	0	0/1	1	1	0/1	2	2	2/3	3	3	2/3	0	0	0/1	0/1	2	2	2/3	2/3	0	0	0/1	0/1	2	2	2/3	2/3	0	1	2	3
Functionality	Acquisition path‡	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_12	TTL_AUX_IO_13	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_28	TTL_AUX_IO_29	TTL_AUX_IO_30	OPTO_AUX_IN0	OPTO_AUX_IN1	OPTO_AUX_IN8	OPTO_AUX_IN9	OPTO_AUX_IN16	OPTO_AUX_IN17	OPTO_AUX_IN24	OPTO_AUX_IN25	LVDS_AUX_IN2	LVDS_AUX_IN3	LVDS_AUX_IN10	LVDS_AUX_IN11	LVDS_AUX_IN18	LVDS_AUX_IN19	LVDS_AUX_IN26	LVDS_AUX_IN27	LVDS_AUX_OUT7	LVDS_AUX_OUT15	LVDS_AUX_OUT23	LVDS_AUX_OUT31
Timer (M_TIMER*n*†)	0		1	2																										1/2			
	1					1	2																								1/2		
	2								1	2																						1/2	
	3											1	2																				1/2
Trigger controller affected by input signal§	0	T0	T1	T2			T3							T0	T1	T2	T3					T0	T1	T2	T3								
	1			T2	T0	T1	T3									T0/ T2	T1/ T3							T0/ T2	T1/ T3								
	2							T0	T1	T2			T3					T0	T1	T2	T3					T0	T1	T2	T3				
	3									T2	T0	T1	T3							T0/ T2	T1/ T3							T0/ T2	T1/ T3				
Timer-clock input	0																						0										
	1																								0								
	2																										0						
	3																												0				
Bit of quadrature input**	0																					0	1										
	1																							0	1								
	2																									0	1						
	3																											0	1				
User output (bit of main static-user-output register M_USER_BIT*n*†)	0	2	3	4			5																							0			
	1			4	2	3	5																								0		
	2							2	3	4			5																			0	
	3									4	2	3	5																				0

*. Matrox Radient eCL-DB does not have this connector.

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Only Matrox Radient eCL-QB has four acquisition paths. For Matrox Radient eCL-DB, only information for acquisition path 0 and 1 is applicable.

§. Note that there are only 4 trigger controllers per acquisition path.

**. A rotary encoder with quadrature output transmits a two-bit code. The table entries 0 and 1, therefore, denote bit position.

Type of signal	Acquisition path	LVDS cam. ctrl															
		CL connect. 0				CL connect. 1				CL connect. 2				CL connect. 3			
		CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4
VSYNC output	0	1	1	1	1												
	1					1	1	1	1								
	2									1	1	1	1				
	3													1	1	1	1
HSYNC output	0	1	1	1	1												
	1					1	1	1	1								
	2									1	1	1	1				
	3													1	1	1	1
Clock output	0	1	1	1	1												
	1					1	1	1	1								
	2									1	1	1	1				
	3													1	1	1	1

The following table lists the auxiliary input signals (or auxiliary I/O signals set to input) that can be rerouted onto output signals and the output signals onto which they can be rerouted.

			LVDS cam. ctrl																TTL Aux I/O												LVDS Aux Out			
			Camera Link Connector 0				Camera Link Connector 1				Camera Link Connector 2				Camera Link Connector 3				Aux I/O Connector												Aux I/O Connector			
																			A			C			B*			D			A	C	B*	D
M_AUX_IO*x* or M_CC_IO*y* for M_DEV*z*†		x																	8	9	2	8	9	3	8	9	2	8	9	3	12	12	13	13
		y	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4																
		z	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3	0	0	0/1	1	1	0/1	2	2	2/3	3	3	2/3	0	1	2	3
Auxiliary input signal (or auxiliary I/O signal set to input)	**M_AUX_IOx**	**Acquisition path**	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_12	TTL_AUX_IO_13	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_28	TTL_AUX_IO_29	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT15	LVDS_AUX_OUT23	LVDS_AUX_OUT31
TTL_AUX_IO_4	8	0	•	•	•	•																												
TTL_AUX_IO_5	9	0																																
TTL_AUX_IO_6	2	0/1	•	•	•	•	•	•	•	•																								
TTL_AUX_IO_12	8	1					•	•	•	•																								
TTL_AUX_IO_13	9	1																																
TTL_AUX_IO_14	3	0/1																																
TTL_AUX_IO_20*	8	2									•	•	•	•																				
TTL_AUX_IO_21*	9	2																																
TTL_AUX_IO_22*	2	2/3									•	•	•	•	•	•	•	•																
TTL_AUX_IO_28	8	3													•	•	•	•																
TTL_AUX_IO_29	9	3																																
TTL_AUX_IO_30	3	2/3																																

		LVDS cam. ctrl																TTL Aux I/O												LVDS Aux Out			
		Camera Link Connector 0				Camera Link Connector 1				Camera Link Connector 2				Camera Link Connector 3				Aux I/O Connector												Aux I/O Connector			
																		A			C			B*			D			A	C	B*	D
M_AUX_IOx or M_CC_IOy for M_DEVz†	x																	8	9	2	8	9	3	8	9	2	8	9	3	12	12	13	13
	y	1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4																
	z	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3	0	0	0/1	1	1	0/1	2	2	2/3	3	3	2/3	0	1	2	3
Auxiliary input signal (or auxiliary I/O signal set to input)	**M_AUX_IOx**	**Acquisition path**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_12	TTL_AUX_IO_13	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_28	TTL_AUX_IO_29	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT15	LVDS_AUX_OUT23	LVDS_AUX_OUT31
OPTO_AUX_IN0	6	0																															
OPTO_AUX_IN1	7	0	•	•	•	•																											
OPTO_AUX_IN8	0	0/1					•	•	•	•																							
OPTO_AUX_IN9	1	0/1	•	•	•	•	•	•	•	•																							
OPTO_AUX_IN16	6	2																															
OPTO_AUX_IN17	7	2									•	•	•	•																			
OPTO_AUX_IN24	0	2/3													•	•	•	•															
OPTO_AUX_IN25	1	2/3									•	•	•	•	•	•	•	•															
LVDS_AUX_IN2	10	0	•	•	•	•																											
LVDS_AUX_IN3	11	0																															
LVDS_AUX_IN10	4	0/1					•	•	•	•																							
LVDS_AUX_IN11	5	0/1	•	•	•	•	•	•	•	•																							
LVDS_AUX_IN18‡	10	2									•	•	•	•																			
LVDS_AUX_IN19‡	11	2																															
LVDS_AUX_IN26	4	2/3													•	•	•	•															
LVDS_AUX_IN27	5	2/3									•	•	•	•	•	•	•	•															

*. Matrox Radient eCL-DB does not have this connector or signal.

†. MIL constant, where *x*, *y*, and *z* correspond to the numbers in the row. M_DEV*z* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Matrox Radient eCL-DB does not have this signal.

Camera control and auxiliary signals for Matrox Radient eCL-SF and eCL-DF

The following tables summarize the auxiliary functionality that the PSGs support, and the corresponding signals that the PSGs can receive/generate, for Matrox Radient eCL-SF and eCL-DF. The table also documents the MIL constants to use.

		LVDS cam. ctrl				LVDS cam. ctrl			
		Camera Link Connector 0				Camera Link Connector 2*			
M_CC_IO*n*	n	1	2	3	4	1	2	3	4
for M_DEV*m*†	m	0	0	0	0	1	1	1	1
Functionality	Acquisition path	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4
Timer (M_TIMER*n*†)	0	1/2	1/2	1/2	1/2				
	1					1/2	1/2	1/2	1/2
User output (bit of Camera Link static-user-output register M_USER_BIT_CC_IO*n*†)	0	0/1	0/1	0/1	0/1				
	1					0/1	0/1	0/1	0/1

*. Only available on Matrox Radient eCL-DF.

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

		TTL Aux I/O								OPTO Aux In								LVDS Aux In								LVDS Aux Out	
		Aux I/O Connector								Aux I/O Connector								Aux I/O Connector								Aux I/O Connector	
		A		C		B*		D		A		C		B*		D		A		C		B*		D		A	B*
M_AUX_IO*n* for M_DEV*m*†	n	8	9	2	3	8	9	2	3	6	7	0	1	6	7	0	1	10	11	4	5	10	11	4	5	12	13
	m	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	1
Functionality	Acquisition path‡	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_30	OPTO_AUX_IN0	OPTO_AUX_IN1	OPTO_AUX_IN8	OPTO_AUX_IN9	OPTO_AUX_IN16	OPTO_AUX_IN17	OPTO_AUX_IN24	OPTO_AUX_IN25	LVDS_AUX_IN2	LVDS_AUX_IN3	LVDS_AUX_IN10	LVDS_AUX_IN11	LVDS_AUX_IN18	LVDS_AUX_IN19	LVDS_AUX_IN26	LVDS_AUX_IN27	LVDS_AUX_OUT7	LVDS_AUX_OUT23
Timer (M_TIMER*n*†)	0		1	2																						1/2	
	1						1	2																			1/2
Trigger controller affected by input signal§	0	T0	T1	T2	T3					T0	T1	T2	T3					T0	T1	T2	T3						
	1					T0	T1	T2	T3					T0	T1	T2	T3					T0	T1	T2	T3		
Timer-clock input	0																		0								
	1																						0				
Bit of quadrature input**	0																	0	1								
	1																					0	1				
User output (bit of main static-user-output register M_USER_BIT*n*†)	0	2	3	4	5																					0	
	1					2	3	4	5																		0

*. Matrox Radient eCL-SF does not have this connector.

†. MIL constant, where *n* and *m* correspond to the number in the row. M_DEV*m* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Only Matrox Radient eCL-DF has two acquisition paths. For Matrox Radient eCL-SF, only information for acquisition path 0 is applicable.

§. Note that there are only 4 trigger controllers per acquisition path.

**. A rotary encoder with quadrature output transmits a two-bit code. The table entries 0 and 1, therefore, denote bit position.

Type of signal	Acquisition path	LVDS cam. ctrl							
		CL connect. 0				CL connect. 2			
		CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4
VSYNC output	0	1	1	1	1				
	1					1	1	1	1
HSYNC output	0	1	1	1	1				
	1					1	1	1	1
Clock output	0	1	1	1	1				
	1					1	1	1	1

The following table lists the auxiliary input signals (or auxiliary I/O signals set to input) that can be rerouted onto output signals and the output signals onto which they can be rerouted.

			LVDS cam. ctrl								TTL Aux I/O								LVDS Aux Out	
			Camera Link Connector 0				Camera Link Connector 2				Aux I/O Connector								Aux I/O Connector	
											A			C	B*			D	A	B*
M_AUX_IO*x* or M_CC_IO*y* for M_DEV*z*†	x										8	9	2	3	8	9	2	3	12	13
	y		1	2	3	4	1	2	3	4										
	z		0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	1
Auxiliary input signal (or auxiliary I/O signal set to input)	M_AUX_IO*x*	Acquisition path	CC1	CC2	CC3	CC4	CC1	CC2	CC3	CC4	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT23
TTL_AUX_IO_4	8	0	•	•	•	•														
TTL_AUX_IO_5	9	0																		
TTL_AUX_IO_6	2	0	•	•	•	•														
TTL_AUX_IO_14	3	0																		
TTL_AUX_IO_20*	8	1					•	•	•	•										
TTL_AUX_IO_21*	9	1																		
TTL_AUX_IO_22*	2	1					•	•	•	•										
TTL_AUX_IO_30	3	1																		
OPTO_AUX_IN0	6	0																		
OPTO_AUX_IN1	7	0	•	•	•	•														
OPTO_AUX_IN8	0	0																		
OPTO_AUX_IN9	1	0	•	•	•	•														
OPTO_AUX_IN16	6	1																		
OPTO_AUX_IN17	7	1					•	•	•	•										
OPTO_AUX_IN24	0	1																		
OPTO_AUX_IN25	1	1					•	•	•	•										

			LVDS cam. ctrl								TTL Aux I/O								LVDS Aux Out	
			Camera Link Connector 0				Camera Link Connector 2				Aux I/O Connector								Aux I/O Connector	
											A			C	B*			D	A	B*
M_AUX_IO*x* or M_CC_IO*y* for M_DEV*z*†		x									8	9	2	3	8	9	2	3	12	13
		y	1	2	3	4	1	2	3	4										
		z	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	1
Auxiliary input signal (or auxiliary I/O signal set to input)	**M_AUX_IOx**	**Acquisition path**	**CC1**	**CC2**	**CC3**	**CC4**	**CC1**	**CC2**	**CC3**	**CC4**	TTL_AUX_IO_4	TTL_AUX_IO_5	TTL_AUX_IO_6	TTL_AUX_IO_14	TTL_AUX_IO_20	TTL_AUX_IO_21	TTL_AUX_IO_22	TTL_AUX_IO_30	LVDS_AUX_OUT7	LVDS_AUX_OUT23
LVDS_AUX_IN2	10	0	•	•	•	•														
LVDS_AUX_IN3	11	0																		
LVDS_AUX_IN10	4	0																		
LVDS_AUX_IN11	5	0	•	•	•	•														
LVDS_AUX_IN18‡	10	1					•	•	•	•										
LVDS_AUX_IN19‡	11	1																		
LVDS_AUX_IN26	4	1																		
LVDS_AUX_IN27	5	1					•	•	•	•										

*. Matrox Radient eCL-SF does not have this connector or signal.

†. MIL constant, where *x*, *y*, and *z* correspond to the numbers in the row. M_DEV*z* is the required device number of the digitizer (**MdigAlloc()**) that you must use to access this signal.

‡. Matrox Radient eCL-SF does not have this signal.

Specifications of the auxiliary and camera control signals

Matrox Radient eCL has auxiliary/camera control signals in the following formats:

Signal format	Total # of signals							
	eCL-SF		eCL-DF		eCL-DB		eCL-QB	
	Without cable adapter bracket	With cable adapter bracket	Without cable adapter bracket	With cable adapter bracket	Without cable adapter bracket	With cable adapter bracket	Without cable adapter bracket	With cable adapter bracket
LVDS camera control output signals	4	4	8	8	8	8	16	16
TTL auxiliary input or output (I/O) signals	3	9	6	12	3	9	6	12
Opto-isolated auxiliary input signals	2	6	4	8	2	6	4	8
LVDS auxiliary input signals	2	6	4	8	2	6	4	8
LVDS auxiliary output signals	1	3	2	4	1	3	2	4

When an auxiliary input signal is received in TTL format directly, it will be clamped at a maximum of 5.7 V and at a minimum of -0.7 V to protect the input buffer. Typically, the signal should have a maximum of 5 V and a minimum of 0 V. A signal over 2 V is considered high, while anything less than 0.8 V is considered low.

The opto-isolated auxiliary input signals pass through an opto-coupler, a device that protects the board from outside surges and different ground levels, and allows the frame grabber to be totally isolated. The voltage difference across the positive and negative components of the signal must be between 4.71 V and 9.165 V for logic high, and between -5.0 V and 0.8V for logic low.

You can set the direction of a bidirectional auxiliary I/O signal using the MIL-Lite function **MdigControl**() with **M_IO_MODE**.

You specify the purpose of the camera control and auxiliary signals in the DCF with Matrox Intellicam. You can then program these signals using the MIL-Lite function **MdigControl**() with **M_IO...***, **M_TRIGGER...**, **M_TIMER...***, or **M_ROTARY_ENCODER...**

*. As of MIL 10.

Timers

Each PSG has two timers. These timers can each generate a timer output signal which allows you to control the exposure time and other external events related to the video source (such as a strobe). The timer signals can be output using camera control signals or auxiliary output signals (or auxiliary I/O signals in output mode).

Each PSG has two 24-bit timers (Timer 1 and 2). The timers can count up to 16777215 clock ticks before resetting.

The timers can use one of the following as a clock source:

- **A clock based on an external pixel clock signal.**
- **A clock that is internally generated.** Each timer can use its PSG's clock generator, which can generate a single clock with a programmable frequency of 0.63 to 85 MHz. Timers can only use the clock generator of their own PSG.
- **A clock from an external source.** In this case, you must define the appropriate auxiliary input signal as a timer-clock input; the timer-clock input signal must meet the electrical specification of the auxiliary signal. The same timer-clock input can be used to clock different timers of the same PSG.
- **A clock based on another timer output of the same PSG.** Timer 1 can use a clock based on Timer 2, and Timer 2 can use a clock based on Timer 1.
- **A clock based on the HSYNC or VSYNC signal generated by the PSG.**

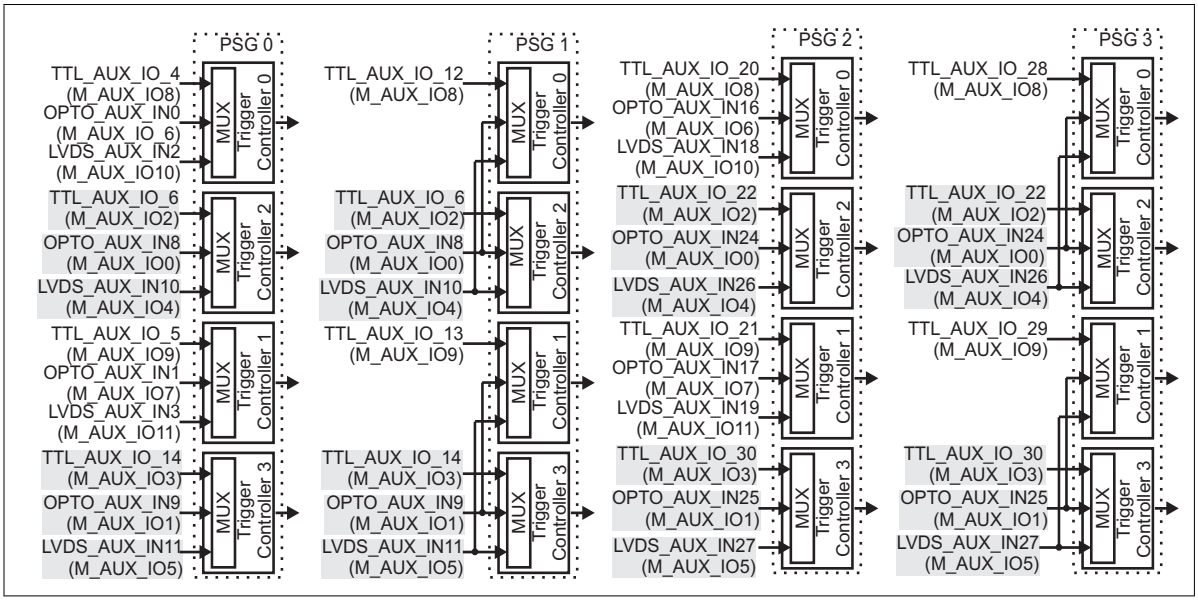
To route a timer output on an auxiliary signal, use the MIL-Lite function **MdigControl**() with **M_IO_SOURCE*** **+ M_AUX_IOn** (or **+ M_CC_IOn**) set to **M_TIMERm***. Set up the timers using **MdigControl**() with **M_TIMER_...**.

*. As of MIL 10.

Trigger

Each PSG has 4 trigger controllers. Each trigger controller can trigger the image acquisition, the timers, and/or the synchronization signals of the PSG's acquisition path. Only one auxiliary signal per trigger controller can be programmed as a trigger input signal.

The auxiliary signals are restricted to specific trigger controllers. The signals are routed to the following trigger controllers:



The trigger input signal must meet the electrical specification of the auxiliary signal.

The trigger signal's pulse width must be greater than two pixels. The same pulse width restriction applies if using the trigger to start a synchronization signal. If using the trigger to start a timer, the trigger signal's pulse width must be greater than two clock periods of the timer. To determine the timer's clock period, take the inverse of the timer's clock frequency. For example, if the pixel frequency is 12.27 MHz, the minimum pulse width is 2 x 1/12.27 MHz (approximately 163 nsec).

To enable grabbing upon a trigger, use the MIL-Lite function **MdigControl**() with **M_GRAB_TRIGGER_STATE***; to set the signal to trigger the grab, use **MdigControl**() with **M_GRAB_TRIGGER_SOURCE***. To start a timer output upon a trigger, use **MdigControl**() with **M_TIMER_TRIGGER_SOURCE***. MIL automatically decides which trigger controller to use based on the selected auxiliary signal and the availability of the trigger controller.

Synchronization

For each PSG, the board can supply one horizontal (HSYNC) and one vertical (VSYNC) synchronization signal to the video source, through the camera control signals. The board also receives synchronization data (frame valid, line valid, and data valid) along with the video data; refer to the Camera Link specification for a description of the synchronization data.

Clock

For each PSG, the board can supply a clock signal to the video source through a camera control signal. The board can also receive a dedicated clock signal.

Rotary decoder

The PSGs of the Matrox Radient eCL board feature a rotary decoder (quadrature decoder). A rotary decoder is used to decode quadrature input received from a rotary encoder with quadrature output. A rotary encoder is a device that provides information about the position and direction of a rotating shaft (for example, that of a conveyor belt). The encoder outputs a two-bit code (also known as Gray code) on two pairs of LVDS wires for each change in position of the rotating shaft; for a given direction of the rotating shaft, the rotary encoder outputs the code in a precise sequence (either 00 - 01 - 11 - 10 or 00 - 10 - 11 - 01, depending on how the rotary encoder is attached to the rotating shaft). If the rotating shaft changes direction, the rotary encoder transmits the Gray code in the reverse sequence (00 - 10 - 11 - 01 or 00 - 01- 11 - 10, respectively).

Upon decoding a Gray code, the rotary decoder increments or decrements its 32-bit internal counter, depending on the direction of movement. You can configure which Gray code sequence represents forward movement and increments the counter; the reverse Gray code sequence will then represent the backward direction and decrement the counter. You can specify the direction of movement occurring when the Gray code sequence is 00 - 01 - 11 - 10, using **MdigControl**() with **M_ROTARY_ENCODER_DIRECTION**.

*. As of MIL 10.

The rotary decoder supports a maximum encoder frequency equal to 1/3 of the pixel clock frequency of the video source. The LVDS receivers of the Matrox Radient eCL board support 5 V rotary encoders.

- Note that an external source must be used to power the rotary encoder (for example, your computer's 5 V power source).

You can configure the rotary decoder's settings, using the MIL-Lite function **MdigControl**() with **M_ROTARY_ENCODER...**, or by modifying the DCF file with Matrox Intellicam.

User signals

Auxiliary signals can also be used to transmit or receive application-specific user output and/or input.

If you want to start or stop an external event based on some calculation or analysis, you can manually set the state of any auxiliary output signal (or I/O signal set to output) to high or low. To do so, you set the state (on/off) of a bit in a user settable register (static-user-output register). When the bit is on, its associated auxiliary output signal will be high; when it is off, the auxiliary output signal will be low. This bit is referred to as a user-bit.

Your application can also act upon and interpret the state of an auxiliary input signal (or I/O signal set to input). The state of an auxiliary input signal is not associated with a user-bit; you poll the state of the signal directly. The state of an auxiliary input signal can also generate an interrupt.

To route the state of a user-bit to an auxiliary output signal, use MdigControl() with **M_IO_SOURCE*** and **M_USER_BITn**; to set the state of a user-bit, use **MdigControl**() with **M_USER_BIT_STATE***. To poll the state of an auxiliary input signal, use **MdigInquire**() with **M_IO_STATUS***; whereas to have the signal cause an interrupt, use **MdigControl**() with **M_IO_INTERRUPT_STATE*** and then use **MdigHookFunction**() with **M_IO_CHANGE*** to hook a function to this event (that is, to set up an event handler).

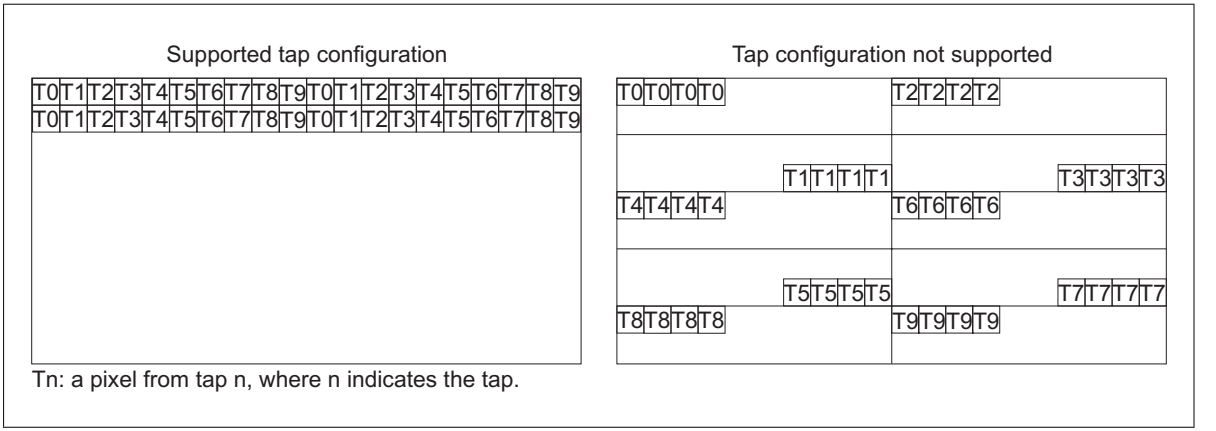
*. As of MIL 10.

Acquisition controller

The acquisition controller is responsible for reconstructing and storing image data in main on-board memory. When writing data to memory, the acquisition controller can perform line and frame reversal; it can flip the image horizontally and/or vertically.

On Matrox Radient eCL-DB/QB, the acquisition controller can write to four non-sequential memory regions (zones) per acquisition path.

On Matrox Radient eCL-SF/DF, the acquisition controller can typically write to eight non-sequential memory regions in single-Medium or single-Full mode, per acquisition path. However, when grabbing 10 taps, the memory controller can only write to one memory region. This means that each of the 10 taps must carry one of 10 sequential pixels



Tn: a pixel from tap n, where n indicates the tap.

Note that the width of each region must be a multiple of the number of taps in that region.

To establish the number of non-sequential memory regions to which your video source must write, refer to the documentation accompanying your video source.

Processing FPGA

To reduce the number of image processing tasks that the Host CPU must perform, Matrox Radient eCL has a Processing FPGA. The Processing FPGA can be configured to offload and even accelerate the most compute-intensive part of typical image processing applications, without generating additional data traffic within the host computer (Host).

Before the Processing FPGA can process grabbed images, they must be stored in main on-board memory. If images stored in Host memory are required, they can be streamed directly to the Processing FPGA for processing. Images resulting from Processing FPGA processing can be stored in main on-board memory or streamed to the Host.

The maximum bandwidth for image streamed directly to/from Host memory is 1 Gbytes/sec, while it is 2 Gbytes/sec for images streamed to/from on-board memory.

Possible processing operations

To use the Processing FPGA, you must configure it with an FPGA configuration that defines the appropriate functionality. An FPGA configuration is a code segment that is used to program an FPGA. You would typically use standard Matrox FPGA configurations. If required, Matrox's FPGA design services can be employed to generate an application-specific FPGA configuration.

Once the Processing FPGA is programmed, you can then make use of its functionality using MIL. Refer to *Using MIL with a Processing FPGA* chapter in the *MIL User Guide* for more information.

FPGA chip

The Processing FPGA on Matrox Radient eCL is implemented using a highly customizable, Altera Stratix III or IV FPGA, with core clock of up to 133 MHz.

Depending on your application requirements, you can purchase the board with one of the following six supported FPGA chips.

	Altera Stratix III package (744 I/Os)					Altera Stratix IV package (744 I/Os)	
	C4 speed grade					C4 speed grade	
	EP3SL150	EP3SL200	EP3SL340	EP3SE110	EP3SE260	EP4SE530	EP4SE820
Equivalent Logic Elements	142,500	200,000	337,500	107,500	255,000	531,200	813,050
Maximum 18x18 multipliers	384	576	576	896	768	1,024	960
M9K memory blocks	355	468	1,040	639	864	1,280	1610
M144K memory blocks	16	36	48	16	48	64	60

Memory

Matrox Radient eCL can have two types of on-board memory:

- **Main on-board memory.** This memory is always present and is used to store acquired images and images for or resulting from processing. As main on-board memory, Matrox Radient eCL uses 2 Gbytes of DDR2-667 SDRAM. Main on-board memory is accessed through the memory controller of the Processing FPGA. The memory controller has multiple input ports and a data transfer rate of up to 10.6 Gbytes/sec.

- **Dedicated Processing FPGA memory (optional).** This memory is optional and is used to store intermediate data while the Processing FPGA performs operations. As Processing FPGA memory, Matrox Radient eCL uses 4 banks of QDR-II SRAM that total 16 or 32 Mbytes of memory and have a total transfer rate of up to 4.0 Gbytes/sec in each direction.

  Use the MIL-Lite functions **MbufAlloc1d**(), **MbufAlloc2d**(), and **MbufAllocColor**() to allocate buffers explicitly in this memory. If you allocate the buffers with the **M_ON_BOARD** attribute, they are allocated in main on-board memory; if you allocate them with the **M_FPGA_ACCESSIBLE+M_FAST_MEMORY** attributes, the buffers are allocated in dedicated Processing FPGA memory.

Host interface

The Matrox Radient eCL Host interface is capable of high-speed DMA transfers to or from Host memory. The DMA read and write engines of the Host interface are capable of performing the transfers without the help of the Host CPU.

Before being transferred off-board, the color space converter and pixel formatter of the Host interface can convert or format the data.

Matrox Radient eCL uses PCIe technology to communicate with the Host. Under optimum conditions, Matrox Radient eCL can exchange data with the Host at a peak transfer rate of up to 2 Gbytes/sec, but can sustain a transfer rate of up to 1750 Mbytes/sec. Optimum conditions include using the board in a PCIe slot with 8 active lanes, using a 256-byte payload. DMA read and write performances are chipset and computer dependent, and are slightly affected by the image size and alignment in Host memory (frame start and line pitch).

The Matrox Radient eCL Host interface actually has four DMA write engines, which can run in parallel; however, only one of these can use the color space converter. The total bandwidth still peaks at 2 Gbytes/sec, but the presence of multiple DMA write engines might help reduce latency.

Color space converter and pixel formatter

The color space converter and pixel formatter can convert data being transferred off-board as follows:

- **Resizing.** Image data can be cropped (ROI capture) and/or subsampled. This can be useful to implement custom software-based motion detection because at a reduced scale, image comparison is faster. The color space converter and pixel formatter can subsample in the horizontal direction by integer factors of 1 to 16; whereas, there is no restriction in the vertical direction; subsampling occurs using nearest-neighbor interpolation.

- **Flipping.** Image data can be flipped vertically.

- **Color space conversion.** Image data can be converted as follows:

In	Out							
	8-bit monochrome	16-bit monochrome	24-bit packed BGR	32-bit packed BGRa	48-bit packed BGR	16-bit YUV (YUYV)	24-bit RGB planar	48-bit RGB planar
8-bit monochrome	yes		yes	yes		yes	yes	
16-bit monochrome	yes	yes	yes	yes	yes	yes	yes	yes
24-bit packed BGR	yes		yes	yes		yes	yes	
48-bit packed BGR	yes	yes	yes	yes	yes	yes	yes	yes

The equations for the YUV16 conversion are described in the following table. The value of *depth* is either 8 or 16 when converting BGR24 or BGR48 data, respectively. Note that while performing BGR48-to-YUV color space conversion, the operations are carried out on 16-bit data; then each resulting YUV component is bit-shifted right by 8 bits (>> (*depth* - 8) where the value of *depth* is 16).

Color space conversion	Equations
BGR-to-YUV	• $Y = (0.114B + 0.587G + 0.299R) >> (depth - 8)$ • $U = (0.500B - 0.331G - 0.169R + 2^{(depth-1)}) >> (depth - 8)$ • $V = (-0.081B - 0.419G + 0.500R + 2^{(depth-1)}) >> (depth - 8)$

Formatting/ converting data when grabbing into Host buffers

When you grab into a Host buffer (for example, using the MIL-Lite function **MdigGrab**()), use **MdigControl**() with **M_SOURCE_OFFSET_X/Y**, **M_SOURCE_SIZE_X/Y**, and/or **M_GRAB_SCALE_X/Y** to crop or resize image data when grabbing.

The color space converter and pixel formatter are not used to flip images grabbed into Host buffers; the acquisition controller is responsible for this task. For more information, see the *Acquisition controller* section, earlier in this chapter. To flip image data when grabbing, use **MdigControl**() with **M_GRAB_DIRECTION_X/Y**.

When grabbing into a Host buffer, the color space converter and pixel formatter automatically converts the bit-depth and color format of the source image to the bit-depth and color format of the destination buffer. The DCF establishes the format of the source, while the destination grab buffer establishes the output format.

Grabbing into on-board buffers

When grabbing into an on-board buffer, only acquisition controller formatting operations are supported; these are horizontal and vertical flipping and, if grabbing from a line-scan video source, cropping in Y. If you transfer image data from an on-board buffer to a Host buffer using the MIL-Lite **MbufCopy**(), **MbufTransfer**(), **MimResize**(), or **MimFlip**() function, any required conversion or formatting operation will be performed using the color space converter and pixel formatter if supported.

To flip image data horizontally in hardware, you must do so while the image is being acquired, using the acquisition controller. When transferring image data from an on-board buffer to a Host buffer, this operation is not supported in hardware.

Appendix A: Glossary

This appendix defines some of the specialized terms used in the Matrox Radient eCL documentation.

Glossary

- **Bandwidth**

  A term describing the capacity to transfer data. Greater bandwidth is needed to sustain a higher transfer rate. Greater bandwidth can be achieved, for example, by using a wider bus or by increasing the clock frequency at which an interface or a core operates (for example, increasing the DDR2 SDRAM clock frequency).

- **Blanking period**

  The portion of a video signal after the end of a line or frame, and before the beginning of a new line or frame. During this period, the video signal is "blank" so that a scan line can be brought back to the beginning of the new line or frame. The portion of a video signal after the end of a line and before the beginning of a new line is known as the *horizontal blanking period*. The portion of a video signal after the end of a frame and before the beginning of a new frame is known as the *vertical blanking period*.

- **Contiguous memory**

  A block of memory occupying a single, unbroken series of addresses.

- **Data valid synchronization signal**

  The signal that indicates the valid pixels in a line (row).

  See also *line valid* and *frame valid synchronization signal*.

- **DCF**

  Digitizer Configuration Format. A file format that defines the input data format and, for example, how to accept or generate video timing signals, such as horizontal sync, vertical sync, and pixel clock.

  Such files have a *.dcf* extension.

- **DDR2 SDRAM**

  Double Data Rate2 Synchronous Dynamic Random Access Memory. A type of memory used for image capture and processing. SDRAM allows Matrox Radient eCL to access data at a very high speed, which is important for I/O-bound functions. This type of memory allows for very high density at low prices, and is very efficient as long as the data is accessed contiguously.

- **Digitizer Configuration Format**

  See DCF.

- **Dynamic range**

  The range of values present in a buffer. An unsigned 8-bit buffer, for example, has an allowable range of 0 to 255; its dynamic range can be any range within these values.

- **Exposure time**

  Refers to the period during which the image sensor of a video source is exposed to light. As the length of this period increases, so does the image brightness.

- **FPGA**

  Field-programmable gate array. An array of digital electronic components that can be programmed to perform a specific function. An FPGA can contain logic gates, lookup tables, flip-flops and programmable interconnect wiring. This combination of customizability and functionality allows for the same FPGA design to be used in a variety of projects.

- **Frame**

  A single image grabbed from a video source.

- **Frame valid synchronization signal**

  The signal that indicates the start and end of a frame.

  See also *data valid* and *line valid synchronization signal*.

- **Grab**

  To acquire an image from a video source.

- **Horizontal blanking period**

  The portion of a video signal after the end of a line and before the beginning of a new line. During this period, the video signal is "blank".

  See also *vertical blanking period*.

- **Latency**

  The time from when a command is sent to when its operation is started.

- **Line valid synchronization signal**

  The signal that indicates the start and end of a line (row).

  See also *data valid* and *frame valid synchronization signal*.

- **LVDS**

  Low-voltage differential signalling. LVDS offers a general-purpose, high bandwidth interface standard for serial and parallel data interfaces that require increased bandwidth at high speed, with low noise and power consumption.

- **Real-time processing**

  The processing of an image as quickly as the next image is grabbed.

  Also known as *live processing*.

- **Rotary encoder**

  A device used to convert the angular position of a shaft or axle to an analog or digital code.

- **Saturate**

  To replace overflows (or underflows) in an operation with the highest (or lowest) possible value that can be held in the destination buffer of the operation.

- **SRAM QDRII**

  Static Random Access Memory Quad Data Rate II. A type of memory used for processing. SRAM allows Matrox Radient eCL to access data at a very high speed, in a random or contiguous manner. The memory interface is actually double data-rate, but is tagged quad data-rate because it has independent read and write ports.

- **Timer output**

  The signal generated by one of the programmable timers of the frame grabber. The timer output can be used to control external hardware. For example, it can be fed to the video source to control its exposure time or used to fire a strobe light.

- **UART**

  Universal Asynchronous Receiver/Transmitter. A component that handles asynchronous communication through a serial interface (for example, RS-232 or LVDS).

- **Vertical blanking period**

  The portion of a video signal after the end of a frame and before the beginning of a new frame. During this period, the video signal is "blank".

  See also *horizontal blanking period*.

Appendix B: Technical information

This appendix contains information that might be useful when installing your Matrox Radient eCL board.

Board summary

Global information

- Operating system: See your software manual for supported versions of Microsoft Windows and Linux.

- Minimum computer requirements:

  - x8 (or x16) PCIe slot*.

  - Processor with an Intel 32-bit or 64-bit architecture, or equivalent.

  - A relatively up-to-date PCIe chipset. The list of platforms that are known to be compatible with Matrox Radient eCL are available on the Matrox website, under the board's PC compatibility list.

  - A proper power supply. Refer to the *Electrical specifications* section.

  Matrox does not guarantee compatibility with all computers that have the above specifications. Please consult with your local Matrox Imaging representative, local Matrox Imaging sales office, the Matrox web site, or the Matrox Imaging Customer Support Group at headquarters before using a specific computer.

Technical features of Matrox Radient eCL

- Matrox Radient eCL-DB has two independent acquisition paths; Matrox Radient eCL-QB has four independent acquisition paths. Each acquisition path supports a video source in the Camera Link Base configuration.

- Matrox Radient eCL-SF has a single acquisition path; Matrox Radient eCL-DF has two acquisition paths. Each acquisition path supports a video source in the Camera Link Medium or Full configuration.

- Processing FPGA. The Processing FPGA can be either an Altera Stratix III FPGA (EP3SL150, EP3SL200, EP3SL340, EP3SE110, or EP3SE260) or an Altera Stratix IV FPGA (EP4SE530 or EP4SE820).

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*. Note that you can also install Matrox Radient eCL in a x4 PCIe slot that has a mechanical x8 connector; however, the maximum transfer rate between Matrox Radient eCL and the Host is reduced by 50%.

- Has a x8 PCIe GEN 1 Host interface.

- Can provide power over Camera Link (PoCL) with SafePower. The PoCL protection on-board fuse can sustain a current of 0.4 A.

- Supports a maximum clock frequency of up to 85 MHz. Clock frequency is also dependent on the length of the cable used. The following are rough guidelines for the maximum clock frequencies that can be achieved; contact your cable manufacturer for the actual maximum clock frequency that can be achieved for your specific cable.

Maximum cable length (m)	Maximum clock frequency (MHz)*
10	70
7	80
5	85

*. Achieved with high quality cables.

- Supports frame and line-scan video sources. The minimum and maximum number of pixels per line are 16 and 65535, respectively.

- During data transfer to Host:

  - Can convert captured or processed 8- or 16-bit monochrome or 24- or 48-bit packed BGR data to monochrome, packed BGR, packed BGRa, planar RGB, or YUV (YUYV) format.

  - Supports line reversal and frame reversal during acquisition. Can only perform frame reversal during data transfer to Host.

  - Can crop (ROI capture) acquired data or subsample it by integer subsampling factors of 1 to 16.

- Has 2 Gbytes of DDR2-667 SDRAM, which it uses as main on-board memory (acquisition and processing). Total memory bandwidth of 10.6 Gbytes/sec.

- Optionally has 4 banks of QDR-II SRAM that total 16 or 32 Mbytes of memory, which it uses as dedicated Processing FPGA memory. Total memory bandwidth of up to 4.0 Gbytes/sec in each direction.

- Has one LVDS serial port (UART) per acquisition path.
- Supports an external 5 V rotary encoder with quadrature output per acquisition path.
- Has four camera control signals (re-routing of specific auxiliary input signals, HSYNC output, VSYNC output, clock output, timer output, or user output) per acquisition path*.
- Has up to 32 auxiliary signals that can be path independent or path dependent, depending on the functionality† selected*. When path dependent, there are:
  - Three TTL auxiliary I/O signals (trigger input or user input, or timer output or user output) per acquisition path.
  - One LVDS auxiliary output signal (timer output or user output) per acquisition path.
  - Two LVDS auxiliary input signals (trigger input, timer-clock input, quadrature input, or user input) per acquisition path.
  - Two opto-isolated auxiliary input signals (trigger input or user input) per acquisition path.

*. See the *Camera control and auxiliary signals for Matrox Radient eCL-DB and eCL-QB* and *Camera control and auxiliary signals for Matrox Radient eCL-SF and eCL-DF* sections in *Chapter 4: Matrox Radient eCL hardware reference* chapter for supported functionality.

†. For example, for Matrox Radient eCL-DB and eCL-QB, TTL_AUX_IO_14 can be used as a trigger input when grabbing from acquisition path 0 or 1; however, you can only route timer 2 of acquisition path 1 to this signal.

Electrical specifications

Matrox Radient eCL (starting from version 002)		
Operating voltage and current (eCL)		Typical: 3.3 V, 850 mA: 2.8 W Typical 12.0 V, 2.4 A: 28.8 W Max. PoCL 12.0 V, 1.6 A: 19.2 W* (Current directly drawn from the slot. Power is not dissipated by the board; it is only used by the camera). Total dissipated by the board: 2.8 W + 28.8 W =31.6 W Total dissipated by board and PoCL camera = 31.6 W + 19.2 W = 50.8 W
I/O Specifications		
	Input signals in LVDS format	100 Ohm differential termination. Input current: -10 µA (min) to +10 µA (max). Common-mode: -4 V (min) to +5 V (max). Differential threshold: low of -50 mV (min); high of +50 mV (max).
	Output signals in LVDS format	No parallel termination. Output current: -10 µA to 10 µA. Output voltage: high (V_{oh}) 1.6 V (max), 1.33 V (typ); low (V_{ol}) 0.9 V (min), 1.02 V (typ) Differential output voltage (with load of 100 Ohm): 250 mV (min) to 450 mV (max). Offset voltage (common-mode): 1.125 V (min) to 1.375 V (max). Propagation delay: 2.8 ns (max).
	Input signals in TTL format	No series termination. Pulled up to 3.3 V with 4.716 k ohm. Clamped to -0.7 V to +5.7 V. Input current: 5 µA (max). Input voltage: low of 0.8 V (max); high of 2.0 V (min).
	Output signals in TTL format	27 Ohm series termination. High-level output current: -32 mA (max). Low-level output current: +64 mA (max). Output voltage: low of 0.55 V (max); high of 2.0 V (min).
	Opto-coupled input signals†	511 Ohm series termination (connected on the anode inputs of the opto-coupler device). Input current: low: 250 µA (max); high: 5 mA (min (thresholded)) to 15 mA (max) (6.3 to 10 mA recommended). Input voltage: low (V_{il}) of 0.8 V (max); high (V_{ih}) of 4.71 V (min) to 9.165 V (max). Input forward voltage (at 25 degrees C): 1.3 V (min), 1.8 V (max). Propagation delay (at 25 degrees C): 100 ns (max).

*. The PoCL protection on-board fuse on Matrox Radient eCL can sustain a current of 0.4 A.

†. The Matrox Radient eCL opto-couplers are manufactured by Agilent or Avago Technologies (P/N HCPL-0631).

Dimensions and environmental specifications

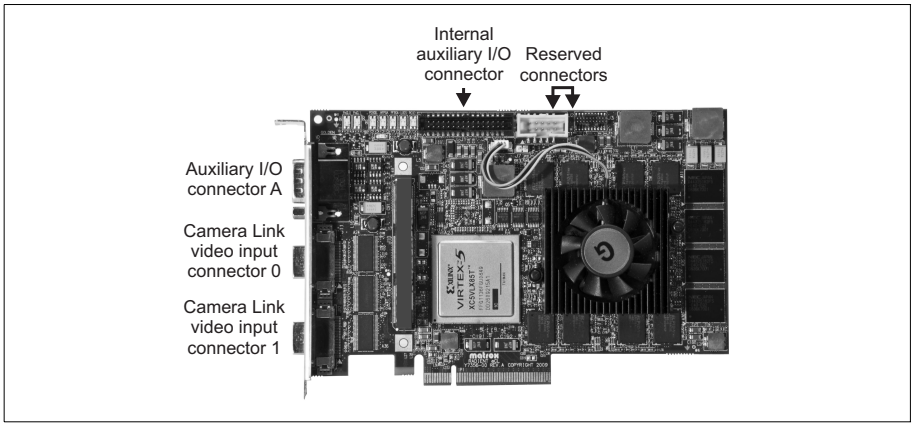
The following dimensions and environmental specifications apply to both Matrox Radient eCL-DB/QB and eCL-SF/DF:

- Dimensions of Matrox Radient eCL-DB and eCL-SF:
  16.76 L x 11.12 H x 1.871 W cm (6.6" x 4.376" x 0.737") from bottom edge of goldfinger to top edge of board.
- Dimensions of Matrox Radient eCL-QB and eCL-DF:
  16.76 L x 11.12 H x 3.903 W cm (6.6" x 4.376" x 1.537") from bottom edge of goldfinger to top edge of board.
- Ventilation: 200 LFM between boards.
- Minimum/maximum ambient operating temperature: 0°C to55°C[*]
  (32°F to 131°F).
- Minimum/maximum storage temperature: -40°C to 75°C (-40°F to 167°F).
- Operating relative humidity: up to 95% relative humidity (non-condensing).
- Storage humidity: up to 95% relative humidity (non-condensing).

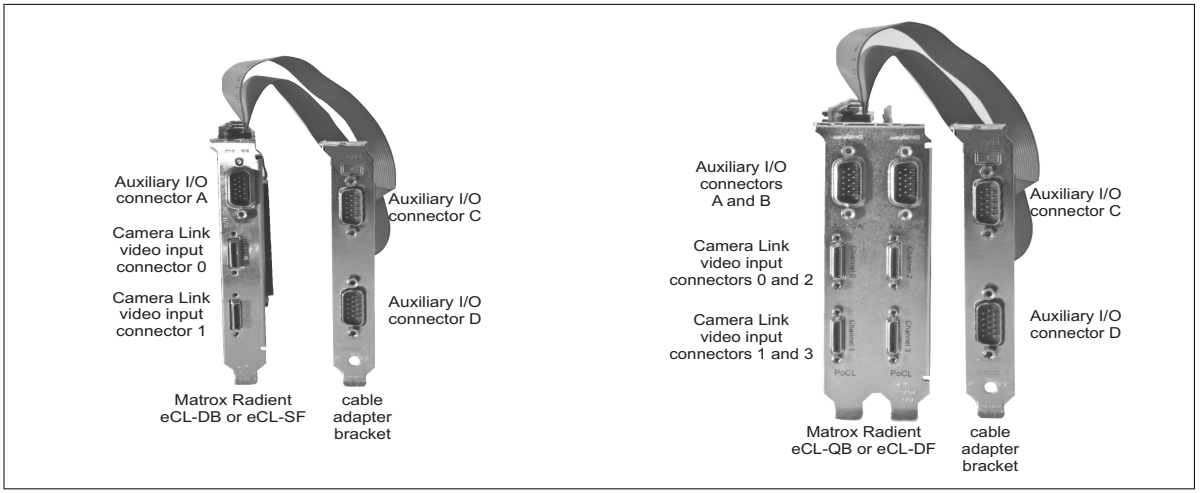
. Up to RAD2G|DF|QB|200432 configuration. Maximum temperature might decrease for larger Processing FPGAs.

Connectors on Matrox Radient eCL boards

On the Matrox Radient eCL boards, there are several interface connectors. On the bracket of Matrox Radient eCL-DB and eCL-SF, there are two Camera Link video input connectors and an auxiliary I/O connector. On the double bracket of Matrox Radient eCL-QB and eCL-DF, there are two pairs of Camera Link video input connectors and two auxiliary I/O connectors. In addition, close to the top edge of the main board, there is an internal auxiliary I/O connector.

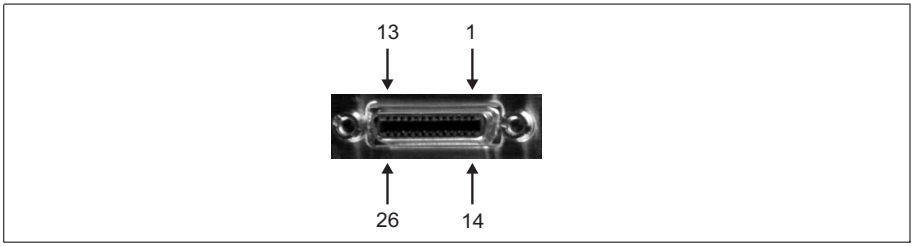


On the Matrox Radient eCL cable adapter bracket, there are two external auxiliary I/O connectors (DBHD-15); these allow you to access the signals of the internal auxiliary I/O connector from outside the computer enclosure.



Camera Link video input connectors

The Camera Link video input connectors are 26-pin high-density female mini Camera Link connectors. They are used to receive video input, timing, and synchronization signals and transmit/receive communication signals between the video source and the frame grabber.



The number of Camera Link video input connectors and their pinout depends on the version of Matrox Radient eCL and the configuration. The pinout of these connectors follows the Camera Link standard.

Matrox Radient eCL-DB and eCL-QB

On Matrox Radient eCL-DB, there are two Camera Link connectors; whereas on Matrox Radient eCL-QB, there are four Camera Link connectors. Each Camera Link connector on Matrox Radient eCL-DB and eCL-QB supports one video source in Base configuration, and has the same pinout; this pinout is listed in the following table.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Description
1	Inner shield		Ground (inner shield), or +12V to camera in PoCL mode.
3+,16-	CC3	M_CC_IO3	Camera control output 3 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals†.
5+,18-	CC1	M_CC_IO1	Camera control output 1 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals†.
6+,19-	SerTFG		Serial port to frame grabber (UART).
8+,21-	X3		Video input data X3.
9+,22-	Xclk		Clock input X.
10+,23-	X2		Video input data X2.
11+,24-	X1		Video input data X1.
12+,25-	X0		Video input data X0.
13	Inner shield		Ground.
14	Inner shield		Ground.
15+,2-	CC4	M_CC_IO4	Camera control output 4 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals†.
17+,4-	CC2	M_CC_IO2	Camera control output 2 for acquisition path n, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEVn), user output (M_USER_BIT_CC_IO0/M_USER_BIT_CC_IO1 on M_DEVn), VSYNC, HSYNC, clock output, or rerouting of specific auxiliary input signals†.
20+,7-	SerTC		Serial port to video source (UART).
26	Inner shield		Ground (inner shield), or +12V to camera in PoCL mode.

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_CCn became represented by M_CC_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

†. See the table in the *Camera control and auxiliary signals* section of *Chapter 4: Matrox Radient eCL hardware reference* for more information on which auxiliary input signals (or auxiliary I/O signals set to input) can be rerouted onto the camera control output signals. Also note that for Matrox Radient eCL-DB and eCL-QB, n should be replaced by the number of the Camera Link connector to which the video source is connected.

Matrox Radient eCL-SF and eCL-DF

On Matrox Radient eCL-SF, there is one pair (0-1) of Camera Link connectors, whereas on Matrox Radient eCL-DF, there are two pairs (0-1 and 2-3) of Camera Link connectors. To each pair of connectors, you can connect one video source in Medium or Full configuration. Each of the connector pairs uses a single acquisition path. In MIL, the (0-1) connector pair uses acquisition path 0 (M_DEV0), and the (2-3) connector pair uses acquisition path 1 (M_DEV1). The top Camera Link connector of each pair has the pinout described above (except replace n with the number of the acquisition path for the connector pair), while the bottom Camera Link connector of each pair has the following pinout.

Warning

❖ When connecting a video source in Full configuration, ensure that you are connecting its cables to the appropriate connector. Accidentally connecting the cables to the wrong connector can damage the board or your video source. Pins 2-5 and pins 15-18 are output pins on the top connector (0 and 2), while they are input pins on the bottom connector (1 and 3).

Pin	Hardware signal name	Description
1	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.
2+, 15-	Z3	Video input data Z3.*
3+, 16-	Zclk	Clock input Z.*
4+, 17-	Z2	Video input data Z2.*
5+, 18-	Z1	Video input data Z1.*
6+, 19-	Z0	Video input data Z0.*
7	terminated	Unused.*
8+, 21-	Y3	Video input data Y3.
9+, 22-	Yclk	Clock input Y.
10+, 23-	Y2	Video input data Y2.
11+, 24-	Y1	Video input data Y1.
12+, 25-	Y0	Video input data Y0.
13	Inner shield	Ground.
14	Inner shield	Ground.
20	100 Ω	Unused.*
26	GND or PWR_OUT	Ground (inner shield), or +12V to camera in PoCL mode.

*. When the board is configured in single-Medium mode, these pins are reserved.

To interface with the above connectors, use a standard Camera Link cable with a 26-pin high-density male mini Camera Link connector (HDR or SDR) at one end. You can purchase such a cable from your video source manufacturer, Components Express inc., 3M Interconnect Solutions for Factory Automation, Intercon 1, or other third parties. Note that this cable is not available from Matrox.

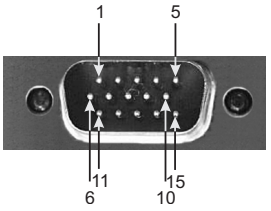
❖ If using both Camera Link connectors to connect to the same video source (Medium configuration or Full configuration), the cables you choose must be of the same type and length. Otherwise, the cables can have different propagation delays.

External auxiliary I/O connectors

The external auxiliary I/O connectors on the Matrox Radient eCL bracket and the cable adapter bracket are high-density D-subminiature 15-pin (DBHD-15*) male connectors; on the cable adapter bracket, the connectors are panel mount connectors. The external auxiliary I/O connectors are used to transmit/receive auxiliary signals.

❖ The auxiliary I/O connectors on Matrox Radient eCL are not compatible with display devices. Connecting one of the DBHD-15 connectors on Matrox Radient eCL to a VGA monitor or any other display device might damage both the device and the Matrox Radient eCL board.

The auxiliary signals can be path independent or path dependent, depending on the functionality selected. For more information, see the *Camera control and auxiliary signals for Matrox Radient eCL-DB and eCL-QB* and *Camera control and auxiliary signals for Matrox Radient eCL-SF and eCL-DF* sections in *Chapter 4: Matrox Radient eCL hardware reference* for supported functionality.



*. Sometimes referred to as DB-15, but more accurately known as DE-15.

Pinouts for auxiliary I/O connectors of Matrox Radient eCL-DB and eCL-QB

The pinout for auxiliary I/O connector A is as follows for Matrox Radient eCL-DB and eCL-QB.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_4	M_AUX_IO8	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: user input, user output (M_USER_BIT2 on M_DEV0), trigger input (trigger controller 0 on acq path 0).
2	TTL_AUX_IO_5	M_AUX_IO9	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: timer output (M_TIMER1 on M_DEV0), trigger input (trigger controller 1 on acq path 0), user input, or user output (M_USER_BIT3 on M_DEV0).
3	TTL_AUX_IO_6	M_AUX_IO2	M_DEV0/ M_DEV1	TTL auxiliary signal (input/output), shared between acquisition paths 0 and 1 for trigger input (trigger control 2 on acq path 0; 2 on acq path 1†), user input, user output (M_USER_BIT4 on M_DEV0/M_DEV1), and dedicated to acquisition path 0 for timer output (M_TIMER2 on M_DEV0).
4+,5-	LVDS_AUX_IN2	M_AUX_IO10	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: trigger input (trigger controller 0 on acq path 0), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN3	M_AUX_IO11	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: user input, trigger input (trigger controller 1 on acq path 0), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN1	M_AUX_IO7	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 1 on acq path 0).
13+,14-	LVDS_AUX_OUT7	M_AUX_IO12	M_DEV0	LVDS auxiliary signal (output) for acquisition path 0, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV0) or user output (M_USER_BIT0 on M_DEV0).
15+,9-	OPTO_AUX_IN0	M_AUX_IO6	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 0 on acq path 0).

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

†. Trigger controller 2 on acq path 1 is only supported on Matrox Radient eCL-DB (for hardware signal TTL_AUX_IO_6).

The pinout for auxiliary I/O connector B is as follows for Matrox Radient eCL-QB.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_20	M_AUX_IO8	M_DEV2	TTL auxiliary signal (input/output) for acquisition path 2, which supports: user input, user output (M_USER_BIT2 on M_DEV2), or trigger input (trigger controller 0 on acq path 2).
2	TTL_AUX_IO_21	M_AUX_IO9	M_DEV2	TTL auxiliary signal (input/output) for acquisition path 2, which supports: timer output (M_TIMER1 on M_DEV2), trigger input (trigger controller 1 on acq path 2), user input, or user output (M_USER_BIT3 on M_DEV2).
3	TTL_AUX_IO_22	M_AUX_IO2	M_DEV2/ M_DEV3	TTL auxiliary signal (input/output), shared between acquisition paths 2 and 3 for trigger input (trigger controller 2 on acq path 2; 2 on acq path 3), user input, user output (M_USER_BIT4 on M_DEV2/M_DEV3), and dedicated to acquisition path 2 for timer output (M_TIMER2 on M_DEV2).
4+,5-	LVDS_AUX_IN18	M_AUX_IO10	M_DEV2	LVDS auxiliary signal (input) for acquisition path 2, which supports: trigger input (trigger controller 0 on acq path 2), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN19	M_AUX_IO11	M_DEV2	LVDS auxiliary signal (input) for acquisition path 2, which supports: user input, trigger input (trigger controller 1 on acq path 2), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN17	M_AUX_IO7	M_DEV2	Opto-isolated auxiliary signal (input) for acquisition path 2, which supports: user input or trigger input (trigger controller 1 on acq path 2).
13+,14-	LVDS_AUX_OUT23	M_AUX_IO12	M_DEV2	LVDS auxiliary signal (output) for acquisition path 2, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV2) or user output (M_USER_BIT0 on M_DEV2).
15+,9-	OPTO_AUX_IN16	M_AUX_IO6	M_DEV2	Opto-isolated auxiliary signal (input) for acquisition path 2, which supports: user input or trigger input (trigger controller 0 on acq path 2).

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

The pinout for auxiliary I/O connector C is as follows for Matrox Radient eCL-DB and eCL-QB.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_12	M_AUX_IO8	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: user input, user output (M_USER_BIT2 on M_DEV1), or trigger input (trigger controller 0 on acq path 1).
2	TTL_AUX_IO_13	M_AUX_IO9	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: timer output (M_TIMER1 on M_DEV1), trigger input (trigger controller 1 on acq path 1), user input, or user output (M_USER_BIT3 on M_DEV1).
3	TTL_AUX_IO_14	M_AUX_IO3	M_DEV0/ M_DEV1	TTL auxiliary signal (input/output), shared between acquisition paths 0 and 1 for trigger input (trigger controller 3 on acq path 0; 3 on acq path 1), user input, user output (M_USER_BIT5 on M_DEV0/M_DEV1), and dedicated to acquisition path 1 for timer output (M_TIMER2 on M_DEV1).
4+,5-	LVDS_AUX_IN10	M_AUX_IO4	M_DEV0/ M_DEV1	LVDS auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 2 on acq path 0; 2 or 0 on acq path 1) or user input, and dedicated to acquisition path 1 for quadrature input bit 0.
6+,8-	LVDS_AUX_IN11	M_AUX_IO5	M_DEV0/ M_DEV1	LVDS auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 1 or 3 on acq path 1; 3 on acq path 0) or user input, and dedicated to acquisition path 1 for timer-clock input or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN9	M_AUX_IO1	M_DEV0/ M_DEV1	Opto-isolated auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 1 or 3 on acq path 1; 3 on acq path 0) or user input.
13+,14-	LVDS_AUX_OUT15	M_AUX_IO12	M_DEV1	LVDS auxiliary signal (output) for acquisition path 1, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV1) or user output (M_USER_BIT0 on M_DEV1).
15+,9-	OPTO_AUX_IN8	M_AUX_IO0	M_DEV0/ M_DEV1	Opto-isolated auxiliary signal (input), shared between acquisition paths 0 and 1 for trigger input (trigger controller 0 or 2 on acq path 1; 2 on acq path 0) or user input.

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

The pinout for auxiliary I/O connector D is as follows for Matrox Radient eCL-QB.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_28	M_AUX_IO8	M_DEV3	TTL auxiliary signal (input/output) for acquisition path 3, which supports: user input, user output (M_USER_BIT2 on M_DEV3), or trigger input (trigger controller 0 on acq path 3).
2	TTL_AUX_IO_29	M_AUX_IO9	M_DEV3	TTL auxiliary signal (input/output) for acquisition path 3, which supports: timer output (M_TIMER1 on M_DEV3), trigger input (trigger controller 1 on acq path 3), user input, or user output (M_USER_BIT3 on M_DEV3).
3	TTL_AUX_IO_30	M_AUX_IO3	M_DEV2/ M_DEV3	TTL auxiliary signal (input/output), shared between acquisition paths 2 and 3 for trigger input (trigger controller 3 on acq path 2; 3 on acq path 3), user input, user output (M_USER_BIT5 on M_DEV2/M_DEV3), and dedicated to acquisition path 3 for timer output (M_TIMER2 on M_DEV3).
4+,5-	LVDS_AUX_IN26	M_AUX_IO4	M_DEV2/ M_DEV3	LVDS auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 0 or 2 on acq path 3; 2 on acq path 2) or user input, and dedicated to acquisition path 3 for quadrature input bit 0.
6+,8-	LVDS_AUX_IN27	M_AUX_IO5	M_DEV2/ M_DEV3	LVDS auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 1 or 3 on acq path 3; 3 on acq path 2) or user input, and dedicated to acquisition path 3 for timer-clock input or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN25	M_AUX_IO1	M_DEV2/ M_DEV3	Opto-isolated auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 1 or 3 on acq path 3; 3 on acq path 2) or user input.
13+,14-	LVDS_AUX_OUT31	M_AUX_IO12	M_DEV3	LVDS auxiliary signal (output) for acquisition path 3, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV3) or user output (M_USER_BIT0 on M_DEV3).
15+,9-	OPTO_AUX_IN24	M_AUX_IO0	M_DEV2/ M_DEV3	Opto-isolated auxiliary signal (input), shared between acquisition paths 2 and 3 for trigger input (trigger controller 0 or 2 on acq path 3; 2 on acq path 2) or user input.

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

Pinouts for auxiliary I/O connectors of Matrox Radient eCL-SF and eCL-DF

The pinout for auxiliary I/O connector A is as follows for Matrox Radient eCL-SF and eCL-DF.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_4	M_AUX_IO8	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: user input, user output (M_USER_BIT2 on M_DEV0), trigger input (trigger controller 0 on acq path 0).
2	TTL_AUX_IO_5	M_AUX_IO9	M_DEV0	TTL auxiliary signal (input/output) for acquisition path 0, which supports: timer output (M_TIMER1 on M_DEV0), trigger input (trigger controller 1 on acq path 0), user input, or user output (M_USER_BIT3 on M_DEV0).
3	TTL_AUX_IO_6	M_AUX_IO2	M_DEV0	TTL auxiliary signal (input/output), for acquisition paths 0, which supports: trigger input (trigger control 2 on acq path 0), user input, user output (M_USER_BIT4 on M_DEV0), or timer output (M_TIMER2 on M_DEV0).
4+,5-	LVDS_AUX_IN2	M_AUX_IO10	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: trigger input (trigger controller 0 on acq path 0), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN3	M_AUX_IO11	M_DEV0	LVDS auxiliary signal (input) for acquisition path 0, which supports: user input, trigger input (trigger controller 1 on acq path 0), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN1	M_AUX_IO7	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 1 on acq path 0).
13+,14-	LVDS_AUX_OUT7	M_AUX_IO12	M_DEV0	LVDS auxiliary signal (output) for acquisition path 0, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV0) or user output (M_USER_BIT0 on M_DEV0).
15+,9-	OPTO_AUX_IN0	M_AUX_IO6	M_DEV0	Opto-isolated auxiliary signal (input) for acquisition path 0, which supports: user input or trigger input (trigger controller 0 on acq path 0).

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

The pinout for auxiliary I/O connector B is as follows for Matrox Radient eCL-DF.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	TTL_AUX_IO_20	M_AUX_IO8	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: user input, user output (M_USER_BIT2 on M_DEV1), or trigger input (trigger controller 0 on acq path 1).
2	TTL_AUX_IO_21	M_AUX_IO9	M_DEV1	TTL auxiliary signal (input/output) for acquisition path 1, which supports: timer output (M_TIMER1 on M_DEV1), trigger input (trigger controller 1 on acq path 1), user input, or user output (M_USER_BIT3 on M_DEV1).
3	TTL_AUX_IO_22	M_AUX_IO2	M_DEV1	TTL auxiliary signal (input/output), for acquisition paths 1 which supports trigger input (trigger controller 2 on acq path 1), user input, user output (M_USER_BIT4 on M_DEV1), and timer output (M_TIMER2 on M_DEV1).
4+,5-	LVDS_AUX_IN18	M_AUX_IO10	M_DEV1	LVDS auxiliary signal (input) for acquisition path 1, which supports: trigger input (trigger controller 0 on acq path 1), user input, or quadrature input bit 0.
6+,8-	LVDS_AUX_IN19	M_AUX_IO11	M_DEV1	LVDS auxiliary signal (input) for acquisition path 1, which supports: user input, trigger input (trigger controller 1 on acq path 1), timer-clock input, or quadrature input bit 1.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN17	M_AUX_IO7	M_DEV1	Opto-isolated auxiliary signal (input) for acquisition path 1, which supports: user input or trigger input (trigger controller 1 on acq path 1).
13+,14-	LVDS_AUX_OUT23	M_AUX_IO12	M_DEV1	LVDS auxiliary signal (output) for acquisition path 1, which supports: timer output (M_TIMER1/M_TIMER2 on M_DEV1) or user output (M_USER_BIT0 on M_DEV1).
15+,9-	OPTO_AUX_IN16	M_AUX_IO6	M_DEV1	Opto-isolated auxiliary signal (input) for acquisition path 1, which supports: user input or trigger input (trigger controller 0 on acq path 1).

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

The pinout for auxiliary I/O connector C is as follows for Matrox Radient eCL-SF and eCL-DF.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	RESERVED			Reserved. Do not connect.
2	RESERVED			Reserved. Do not connect.
3	TTL_AUX_IO_14	M_AUX_IO3	M_DEV0	TTL auxiliary signal (input/output), for acquisition path 0, which supports: trigger input (trigger controller 3 on acq path 0), user input, or user output (M_USER_BIT5 on M_DEV0).
4+,5-	LVDS_AUX_IN10	M_AUX_IO4	M_DEV0	LVDS auxiliary signal (input), for acquisition path 0, which supports: trigger input (trigger controller 2 on acq path 0) or user input.
6+,8-	LVDS_AUX_IN11	M_AUX_IO5	M_DEV0	LVDS auxiliary signal (input), for acquisition path 0, which supports: trigger input (trigger controller 3 on acq path 0) or user input.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN9	M_AUX_IO1	M_DEV0	Opto-isolated auxiliary signal (input), for acquisition path 0,which supports: trigger input (trigger controller 3 on acq path 0) or user input.
13	RESERVED			Reserved. Do not connect.
14	RESERVED			Reserved. Do not connect.
15+,9-	OPTO_AUX_IN8	M_AUX_IO0	M_DEV0	Opto-isolated auxiliary signal (input), for acquisition path 0, which supports: trigger input (trigger controller 2 on acq path 0) or user input.

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

The pinout for auxiliary I/O connector D is as follows for Matrox Radient eCL-DF.

Pin	Hardware signal name	MIL constant for auxiliary signal*	Digitizer device number for auxiliary signal	Description
1	RESERVED			Reserved. Do not connect.
2	RESERVED			Reserved. Do not connect.
3	TTL_AUX_IO_30	M_AUX_IO3	M_DEV1	TTL auxiliary signal (input/output), for acquisition path 1, which supports: trigger input (trigger controller 3 on acq path 1), user input, or user output (M_USER_BIT5 on M_DEV1).
4+,5-	LVDS_AUX_IN26	M_AUX_IO4	M_DEV1	LVDS auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 2 on acq path 1) or user input.
6+,8-	LVDS_AUX_IN27	M_AUX_IO5	M_DEV1	LVDS auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 3 on acq path 1) or user input.
7	GND	N/A	N/A	Ground.
10	GND	N/A	N/A	Ground.
12+,11-	OPTO_AUX_IN25	M_AUX_IO1	M_DEV1	Opto-isolated auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 3 on acq path 1) or user input.
13	RESERVED			Reserved. Do not connect.
14	RESERVED			Reserved. Do not connect.
15+,9-	OPTO_AUX_IN24	M_AUX_IO0	M_DEV1	Opto-isolated auxiliary signal (input), for acquisition path 1, which supports: trigger input (trigger controller 2 on acq path 1) or user input.

*. These MIL constants represent the signals as of MIL 10. The signals that were previously represented by M_HARDWARE_PORTn became represented by M_AUX_IOn (where the value of n remained the same between the constants). For a complete list of changes between previous MIL versions and MIL 10, see *MILRadientCameraLinkIOConversionTable* within *MIL Release Notes*.

To build your own cable, you can purchase the following parts:

	Mating information
Manufacturer:	NorComp, Inc.
Connector:	180-015-203L001
Backshell:	970-015-010-011

These parts can be purchased from third parties such as Digi-Key Corporation (www.digikey.com).

Appendix C: Acknowledgments

This appendix lists the copyright information regarding third-party material used to implement components on the Matrox Radient eCL board.

UART copyright information

The following is the copyright notice for the UART design used on the Matrox Radient eCL boards.

Appendix D: Major revisions of Matrox Radient eCL boards

This appendix lists the major revisions of the Matrox Radient eCL boards.

Major revisions of Matrox Radient eCL

Versions of Matrox Radient eCL		
Part number	**Version**	**Description**
RAD2GSF150400* RAD2GSF150416* RAD2GDB150400* RAD2GDB150416*	000	First shipping version.
	001	Changed inductor value on 5V switcher supply.
	002	Replaced pull-down by pull-up on TTL auxiliary I/O inputs.
	200	Cleaned up PMB, added fan regulation, HFPGA hara-kiri, improved power sequencing.
	201	Added threadlocking adhesive on mini-Camera Link connectors' thumbscrews.
	202	Fixed the PMB to avoid a potential issue powering up the clock generator.
RAD2GDF150400* RAD2GDF200432* RAD2GQB150400* RAD2GQB200432*	000	First shipping version.
	001	Changed inductor value on 5V switcher supply.
	002	Replaced pull-down by pull-up on TTL auxiliary I/O inputs.
	003	No functional change.
	004	Used the new revision of the base-board (version 200).
	005	Added threadlocking adhesive on mini-Camera Link connectors' thumbscrews.
	006	Fixed the PMB to avoid a potential issue powering up the clock generator.

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Regulatory Compliance

FCC Compliance Statement

Warning

Changes or modifications to these units not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

The use of shielded cables for connections of these devices to other peripherals is required to meet the regulatory requirements.

Note

These devices comply with Part 15 of FCC Rules. Operation is subject to the following two conditions:

1. These devices may not cause harmful interference, and
2. These devices must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for Class A digital devices, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of these devices in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

Industry Canada Compliance Statement

These digital apparatuses do not exceed the Class A limits for radio noise emission from digital apparatuses set out in the Radio Interference Regulations of Industry Canada.

Ces appareils numériques n'émettent pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de Classe A prescrites dans le Règlement sur le brouillage radioélectrique édicté par Industrie Canada.

EU Notice (European Union)

WARNING: These are class A products. In a domestic environment these products may cause radio interference in which case the user may be required to take adequate measures.

AVERTISSEMENT: Ces appareils sont des produits informatiques de Classe A. Lorsque ces appareils sont utilisent dans un environnement résidentiel, ces produits peuvent entraîner des interférences radioélectriques. Dans ce cas, l'usager peut être prié de prendre des mesures correctives appropriées.

This device complies with EC Directive 89/336/EEC for Class A digital devices. They have been tested and found to comply with EN55022/CISPR22 and EN55024/CISPR24 when installed in a typical class A compliant host system. It is assumed that these devices will also achieve compliance in any Class A compliant system.

Ces unités sont conformes à la Directive communautaire 89/336/EEC pour les unités numériques de Classe A. Les tests effectués one prouvé qu'elles sont conformes aux normes EN55022/CISPR22 et EN55024/CISPR24 lorsqu'elles sont installées dans un système hôte typique de la Classe A. On suppose qu'ils présenteront la même compatibilité dans tout système compatible de la Classe A.

Directive on Waste Electrical and Electronic Equipment (WEEE)

Europe

(English) European user's information – Directive on Waste Electrical and Electronic Equipment (WEEE)

Please refer to the Matrox Web site (**www.matrox.com/environment/weee**) for recycling information.

(Français) Informations aux utilisateurs Européens – Règlementation des déchets d'équipements électriques et électroniques (DEEE)

Se référer au site Web de Matrox (**www.matrox.com/environment/weee**) pour l'information concernant le recyclage.

(Deutsch) Information für europäische Anwender – Europäische Regelungen zu Elektro- und Elektronikaltgeräten (WEEE)

Bitte wenden Sie sich an dem Matrox-Website (**www.matrox.com/environment/weee**) für Recycling Informationen.

(Italiano) Informazioni per gli utenti europei – Direttiva sui rifiuti di apparecchiature elettriche ed elettroniche (RAEE)

Si prega di riferirsi al sito Web Matrox (**www.matrox.com/environment/weee**) per le informazioni di riciclaggio.

Limited warranty

Refer to the warranty statement that came with your product.